SEC RISC-V Workshop 2020

Call For Papers (CFP)

The first international workshop on Secure RISC-V (SECRISC-V) architecture design exploration seeks original research papers on the design, implementation, verification, and evaluation of micro-architecture security features, hardware-assisted security techniques, and secure executions around the RISC-V instruction set architecture (ISA).

Co-located with ISPASS 2020 - April 5-7, 2020 - Boston, Massachusetts

Submission of early work is encouraged. The RISC-V ISA based topics of specific interest for the workshop include, but are not limited to:

- Secure cores and multicores
- ISA extensions for Security
- Software and hardware obfuscation Techniques
- Secure, efficient, and lightweight hardware implementations
- Hardware security solutions for machine learning
- Secure design for emerging applications: IoT, robotics, wearable computing
- Architectural designs and hardware security solutions for HPC, Data Centers and cloud computing
- Hardware virtualization and isolation for security
- Hardware-Software co-design solutions: graph analytics,
- Post-quantum cryptosystem designs
- Quantum Computing
- Neuromorphic Architectures
- Blockchain enabled secure computing
- Classic and Modern encryption algorithms and hardware support
- Hardware security support for integrity and authentication, key distribution and management, and trust platform modules
- Software and core authentication
- Secure execution environment
- Secure root of trust bios
- Memory subsystem organization to secure data accesses
- Network-on-Chip (NoC) security feature to process and compute isolation

The paper must be submitted in PDF format. The content of the submission is limited to four (4) pages - 8.5"x11" in standard IEEE two-column format (both blind and non-blind submission forms are accepted).

Deadlines

- Submission: February 7, 2020
- Notification: February 28, 2020
- Final Version: March 20, 2020

Website

https://ascslab.org/conferences/secriscv/index.html