SEC RISC-V

Enclave Computing on RISC-V: A Brighter Future for Security?

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First International Workshop on Secure RISC-V Architecture Design Exploration (SECRISC-V‘20)

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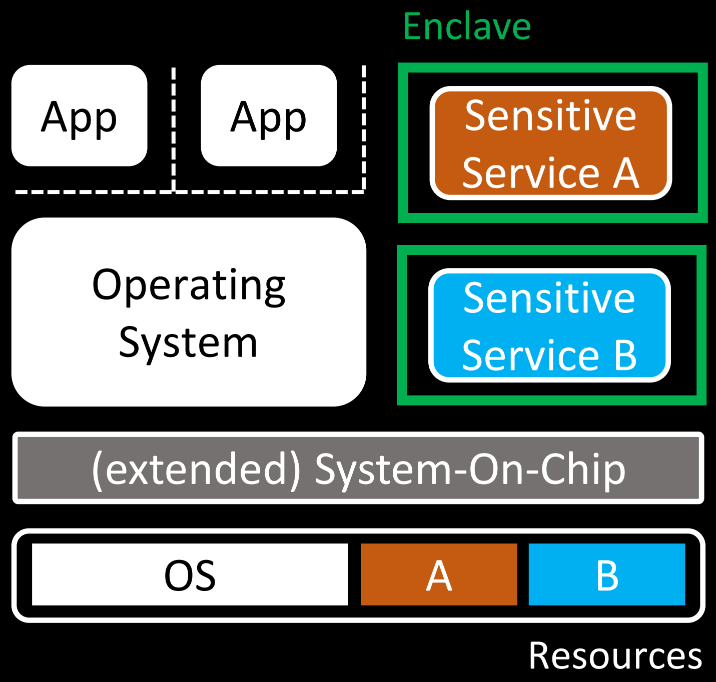

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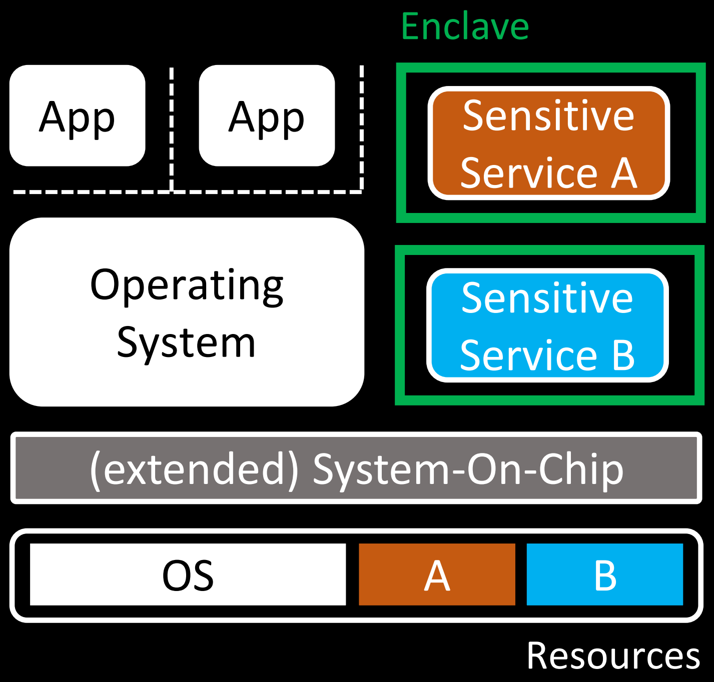

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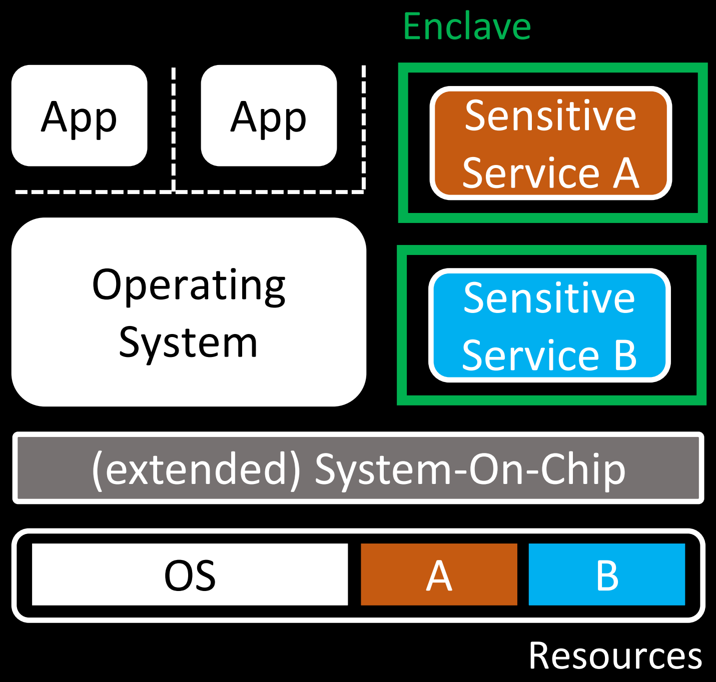

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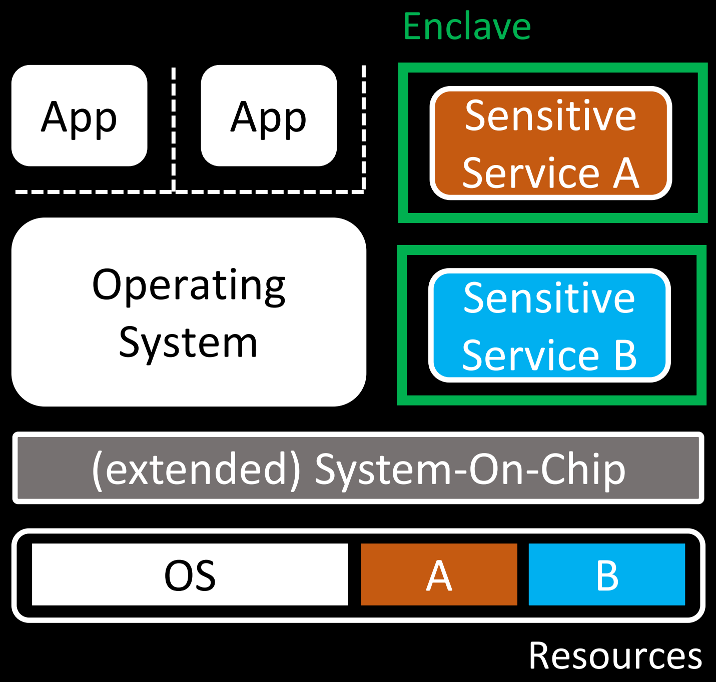

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- Open HW concept of RISC-V propels research on enclave computing

Enclave Security Architectures on RISC-V

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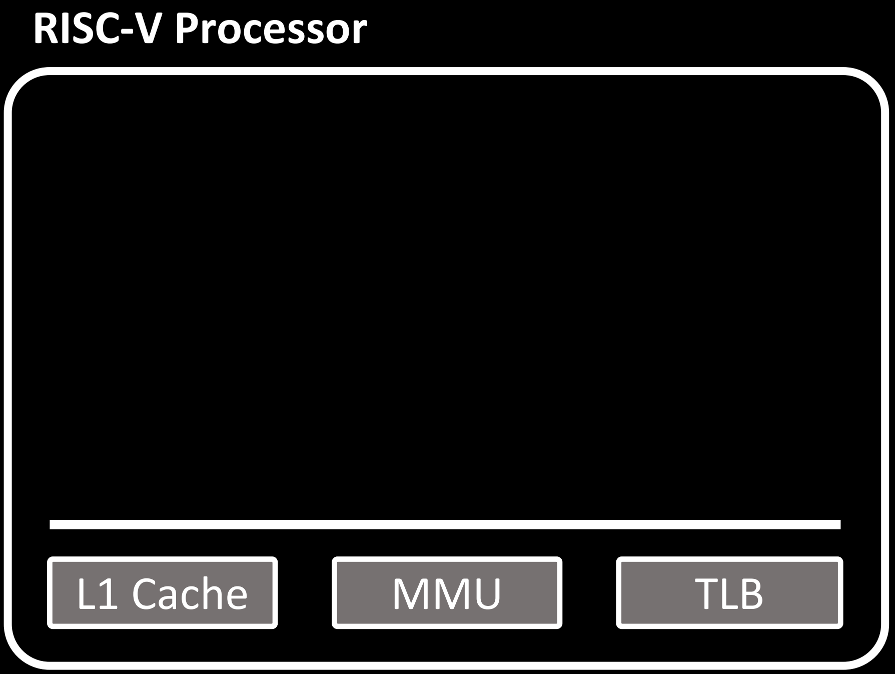

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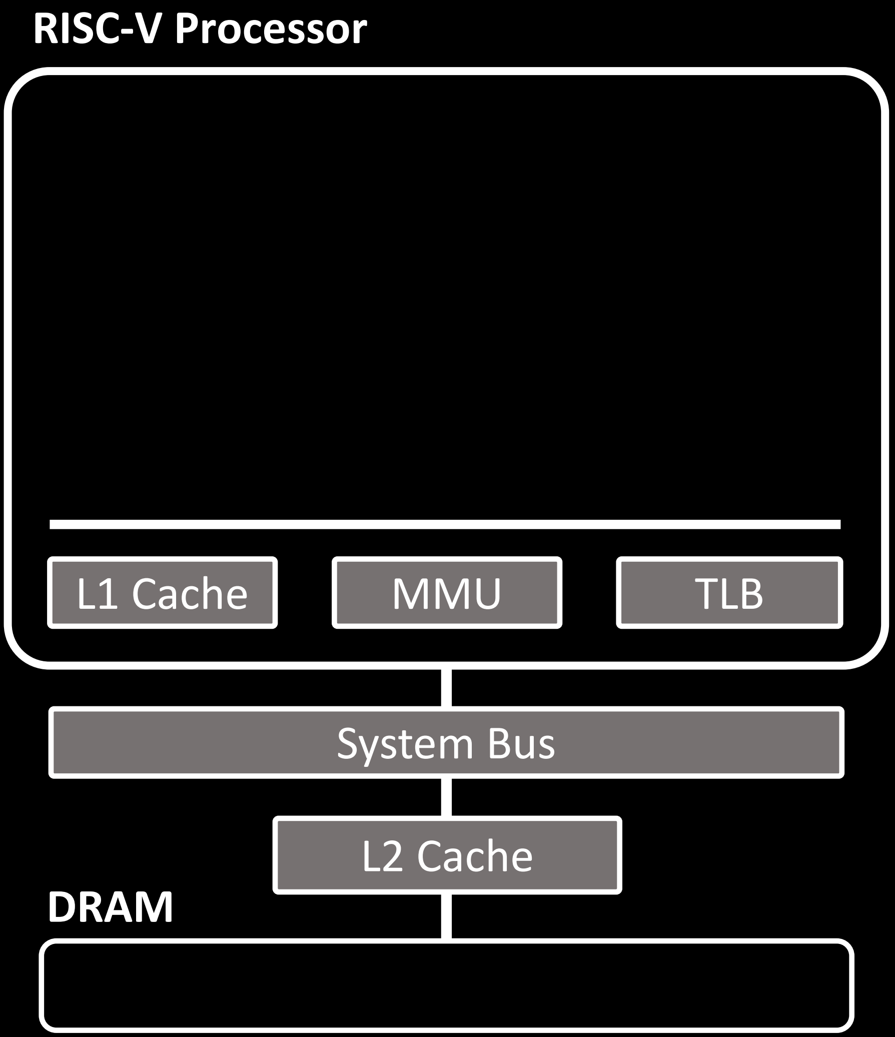

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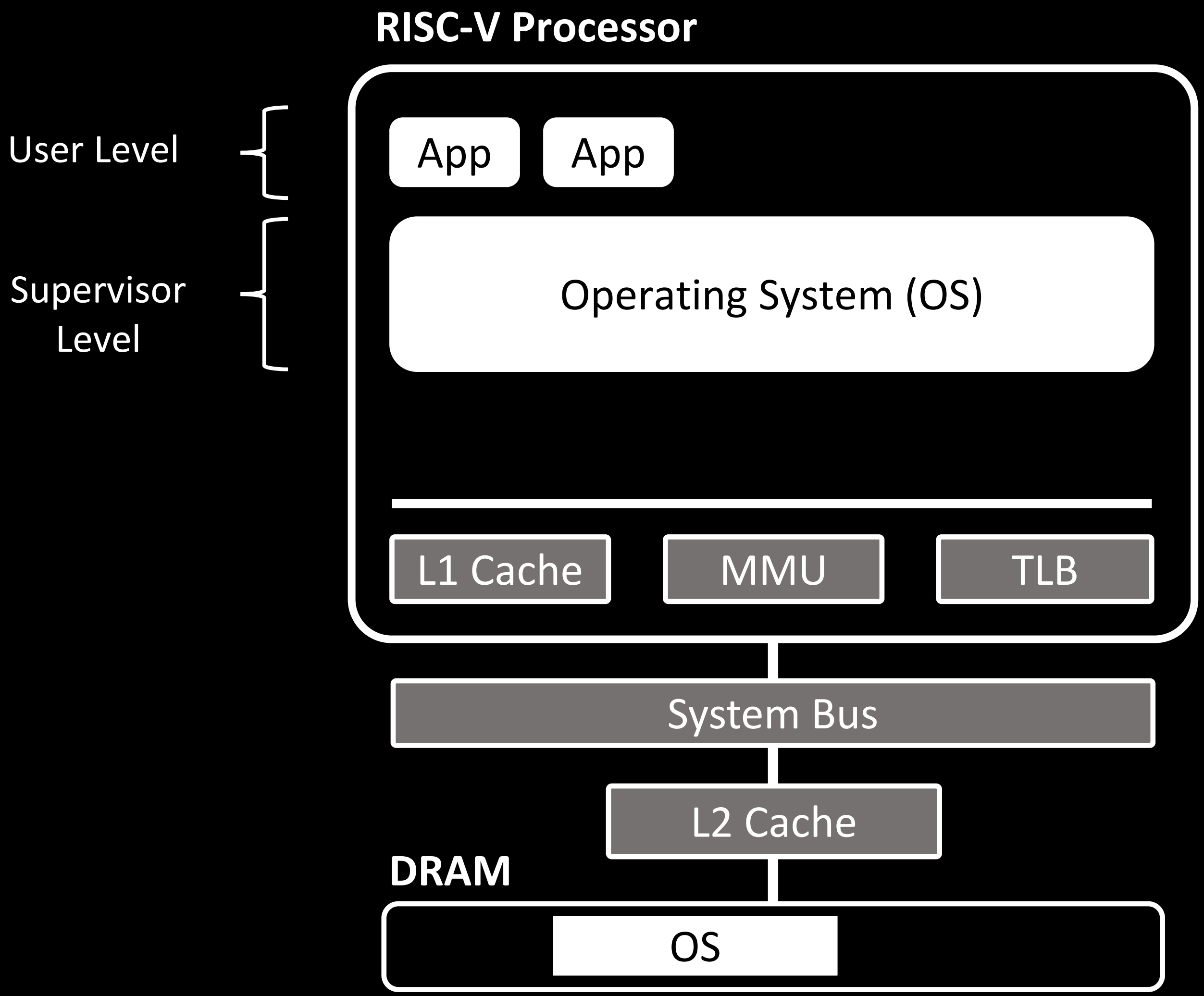

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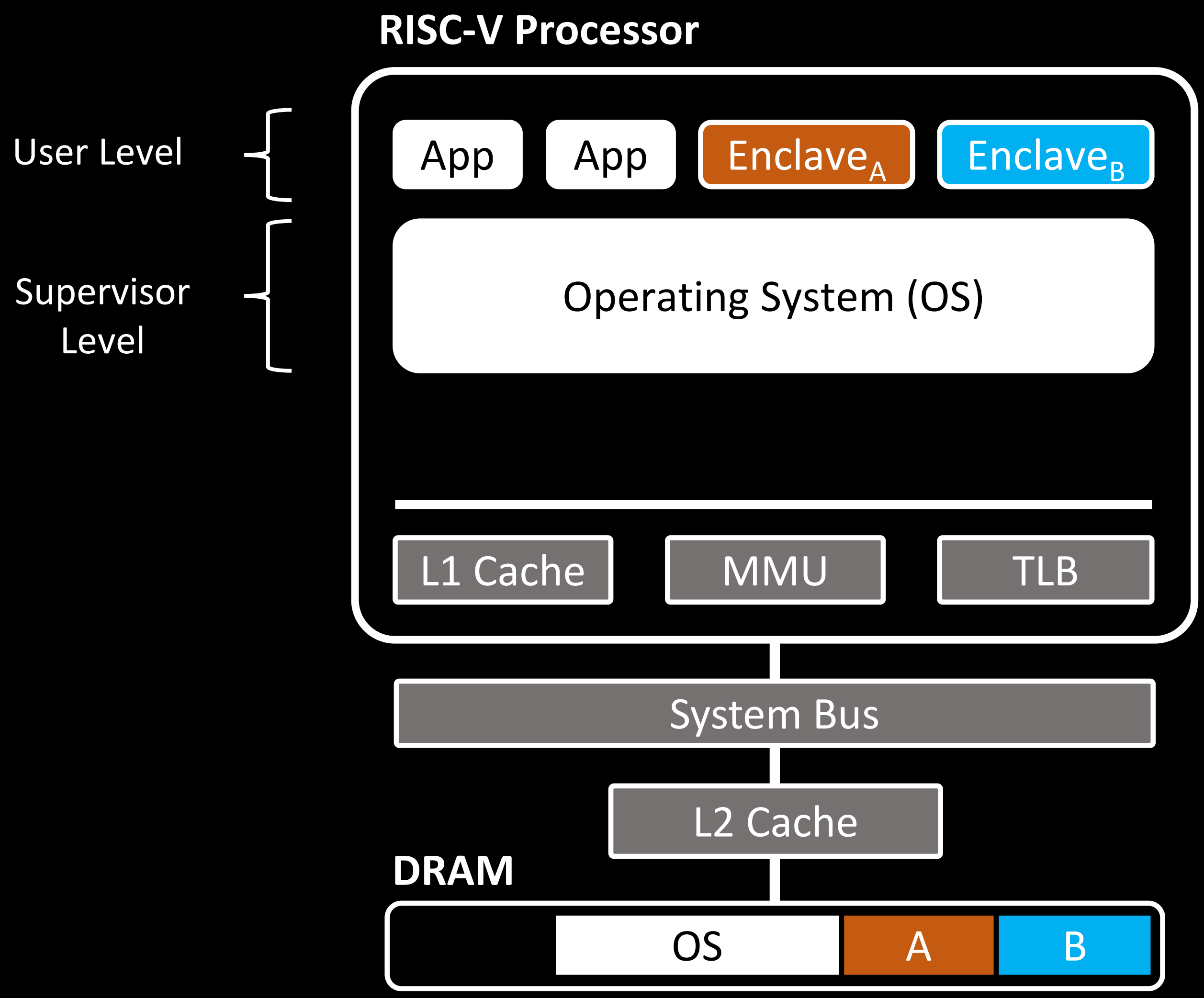

- Enclaves in user level

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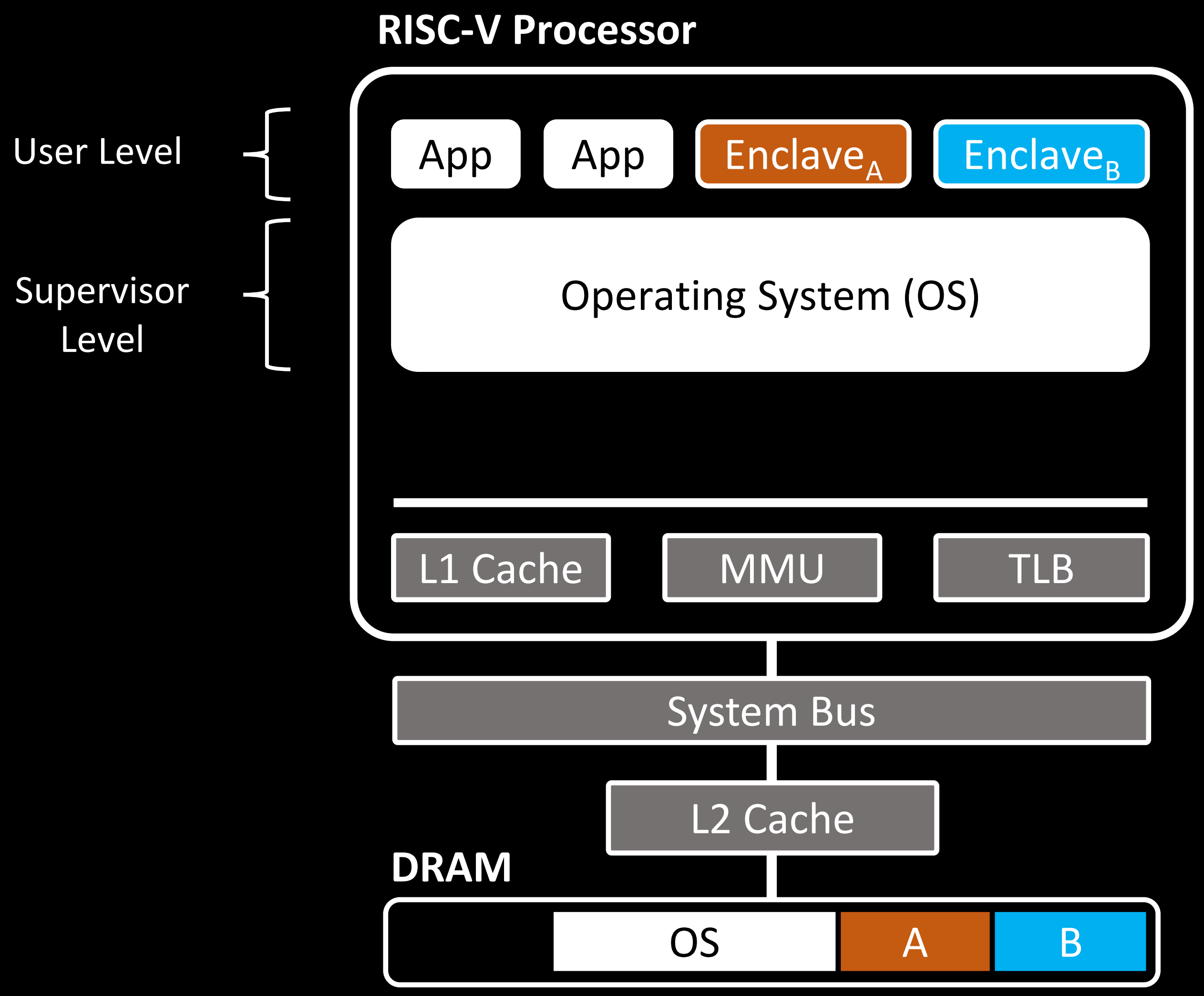

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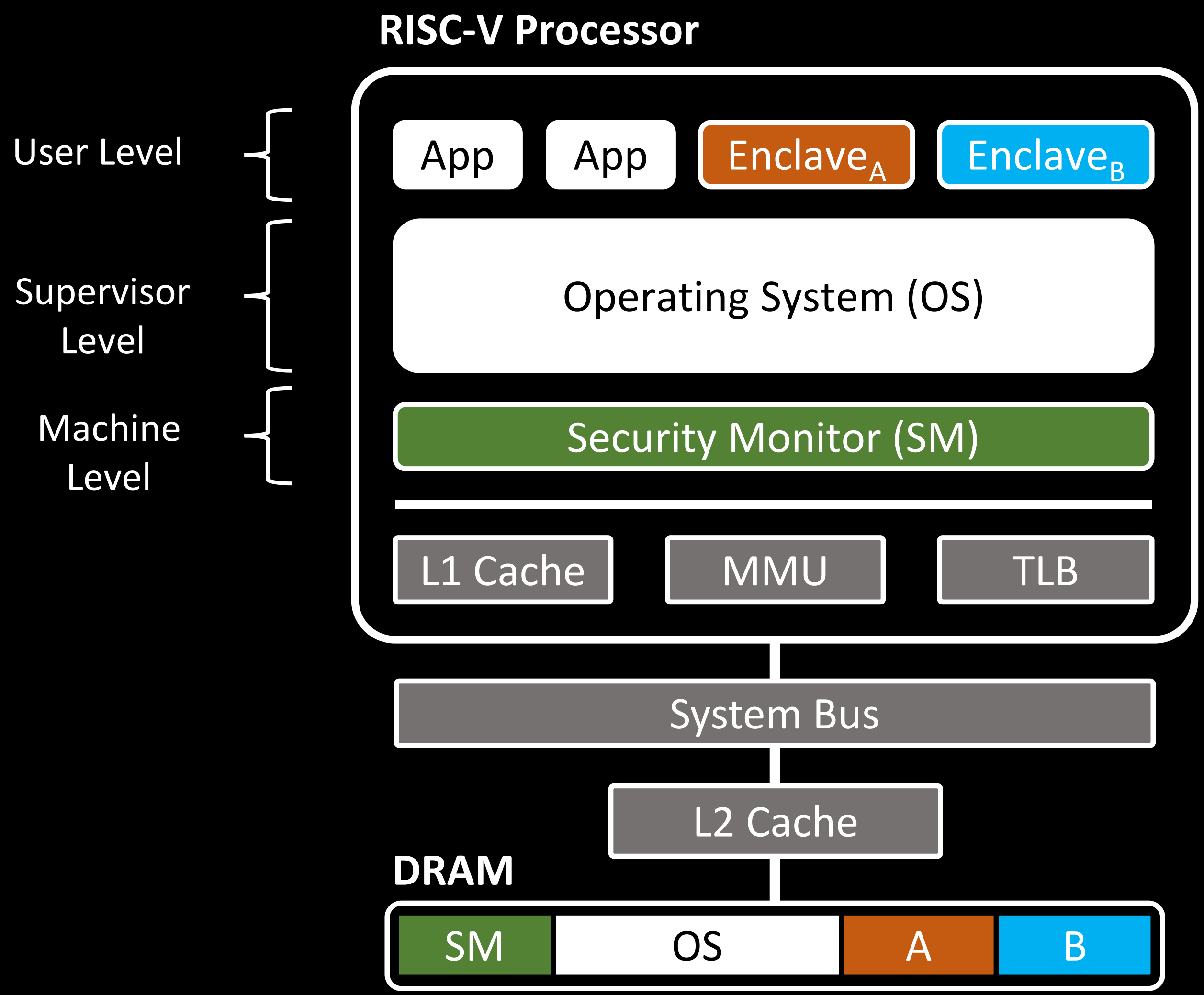

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🟩 Software TCB

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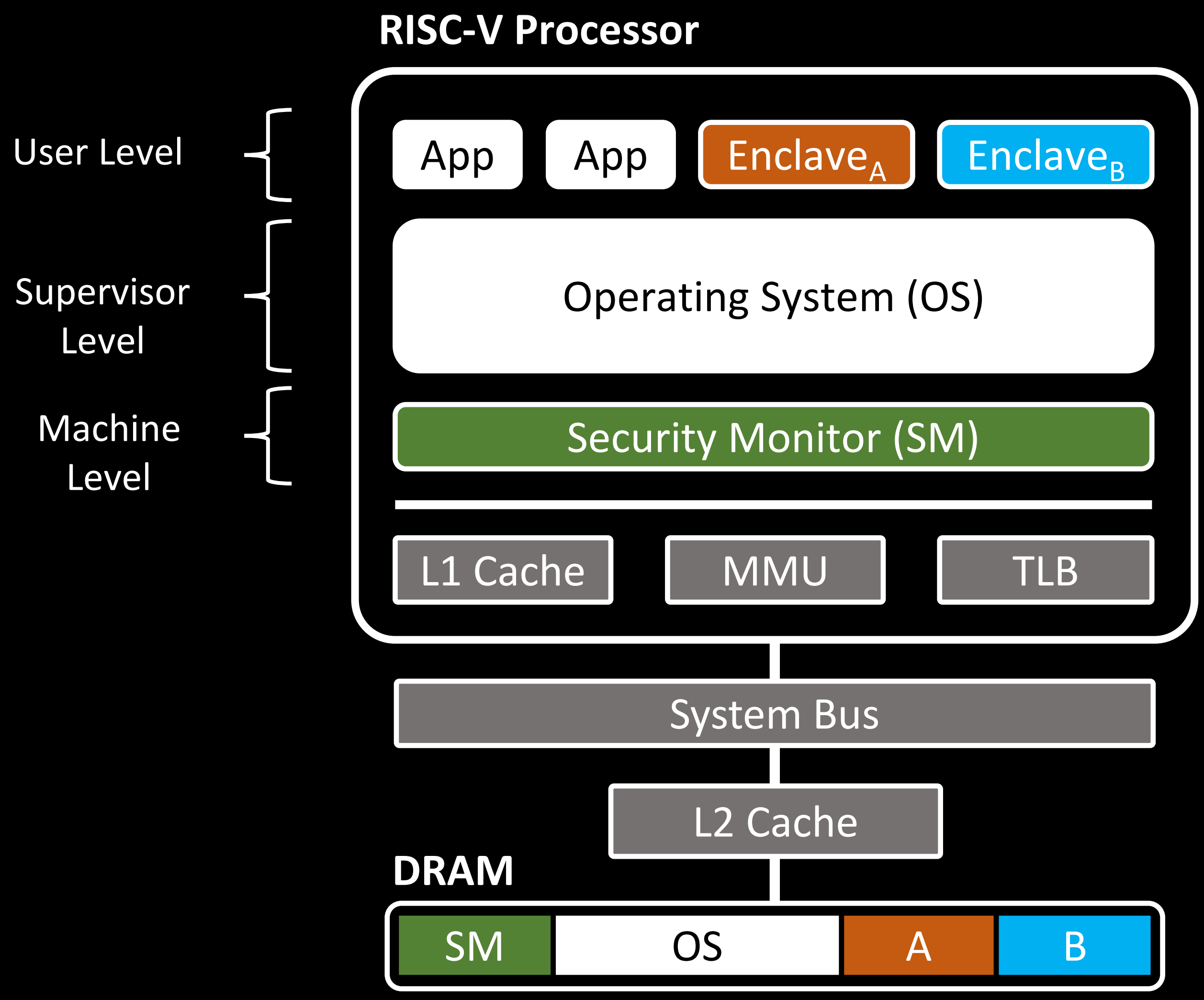

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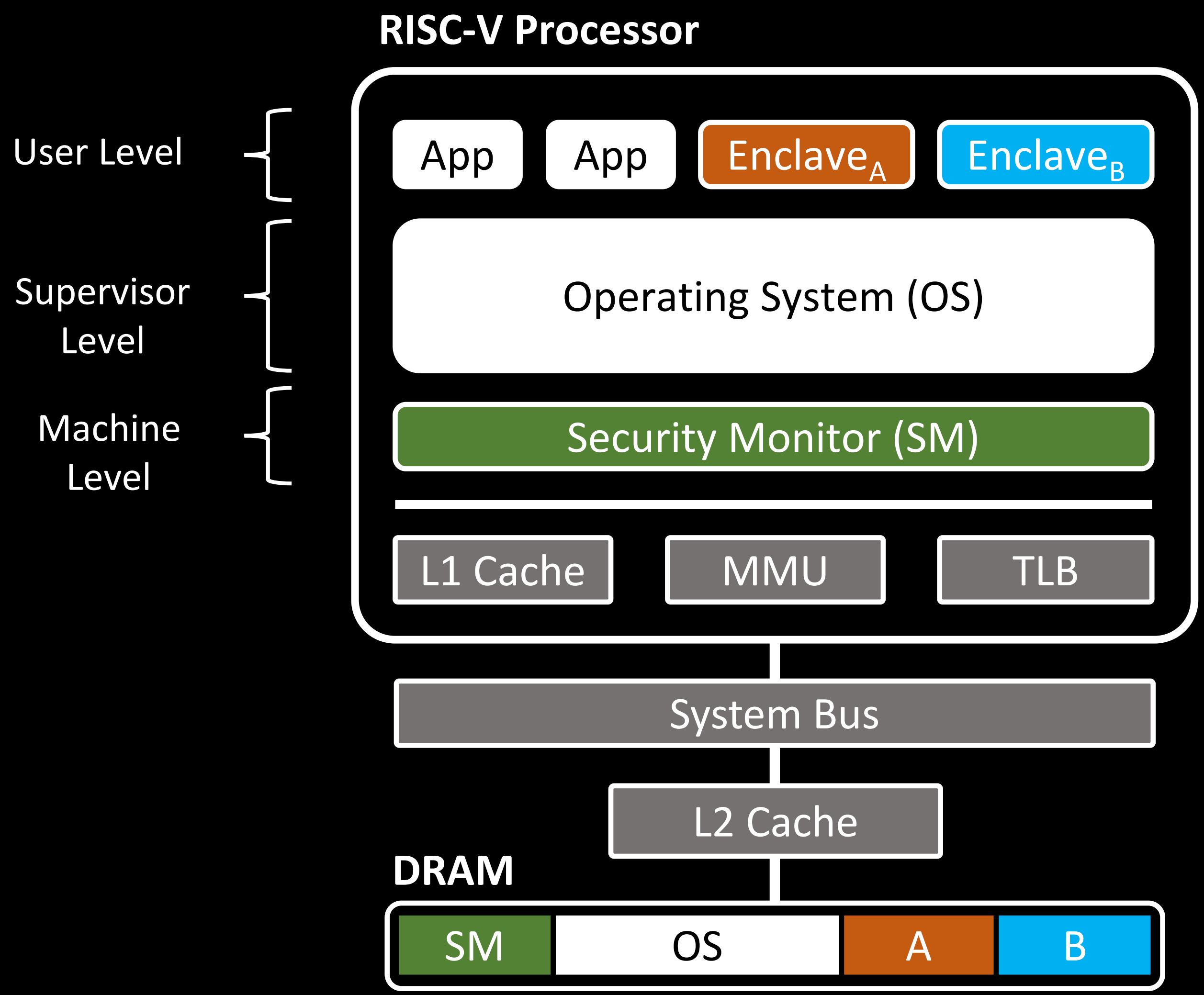

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- Cache side-channel protection through page coloring, influences OS memory layout

🟩 Software TCB

[Lee et al., EuroSys 2020]

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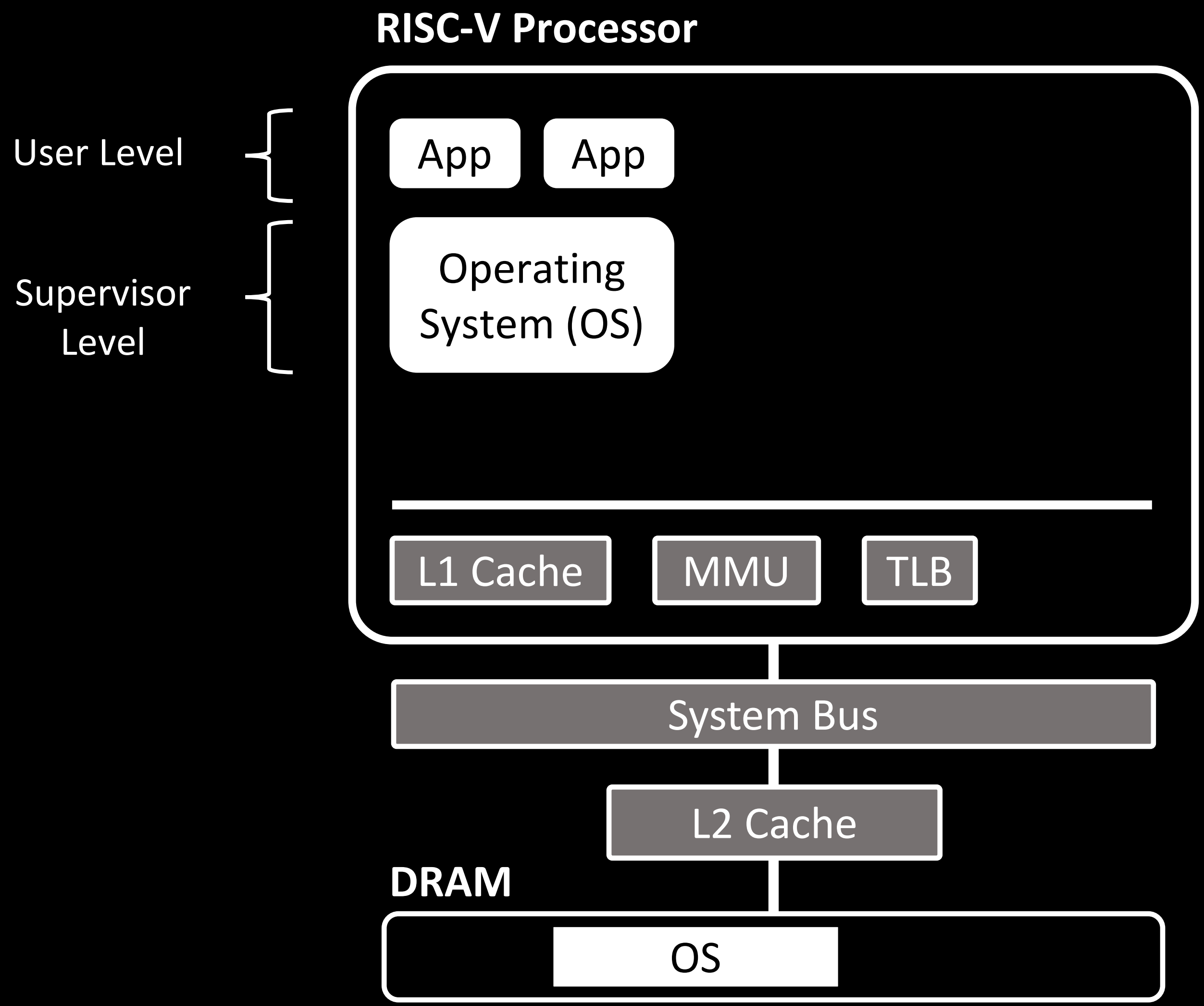

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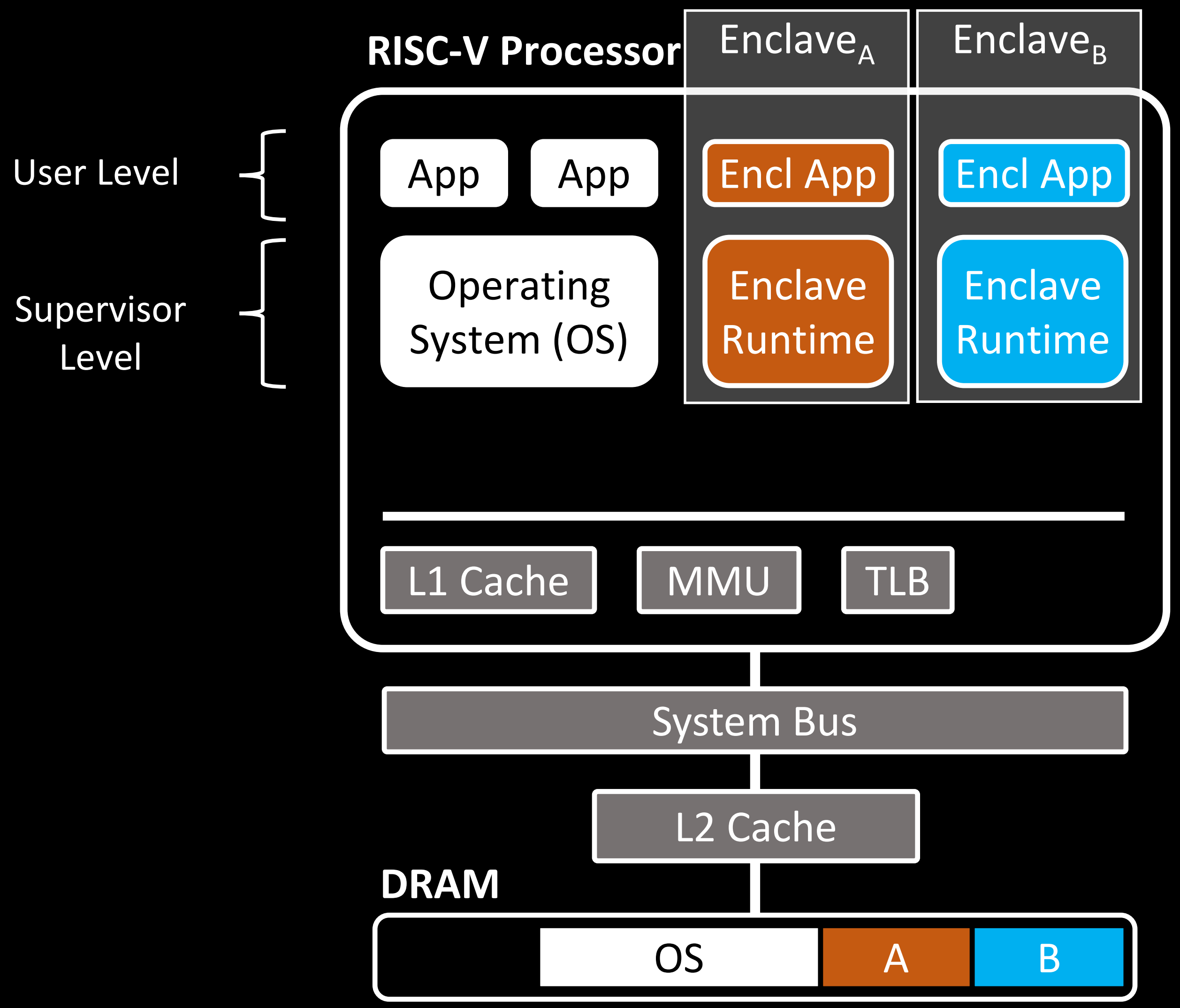

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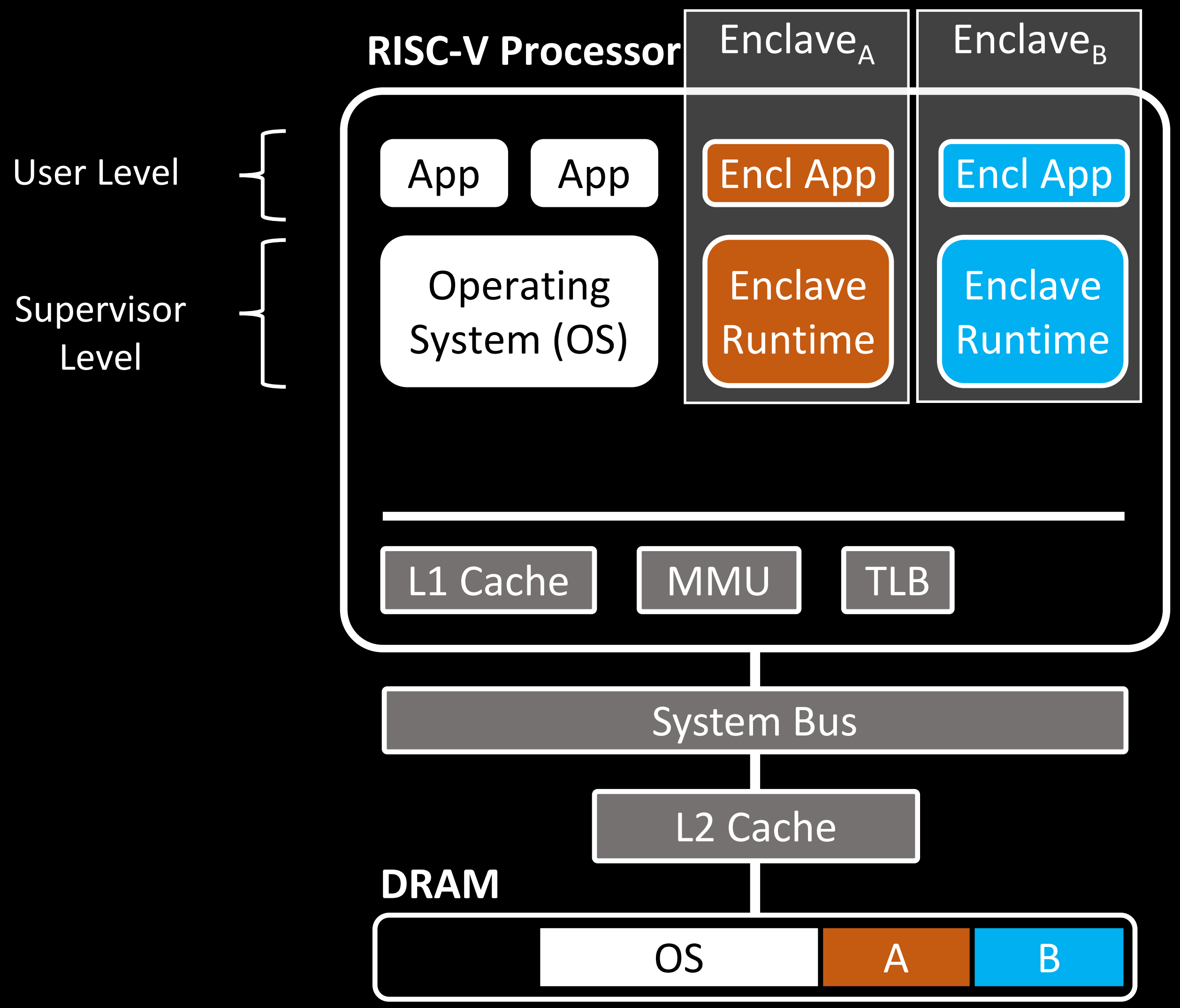

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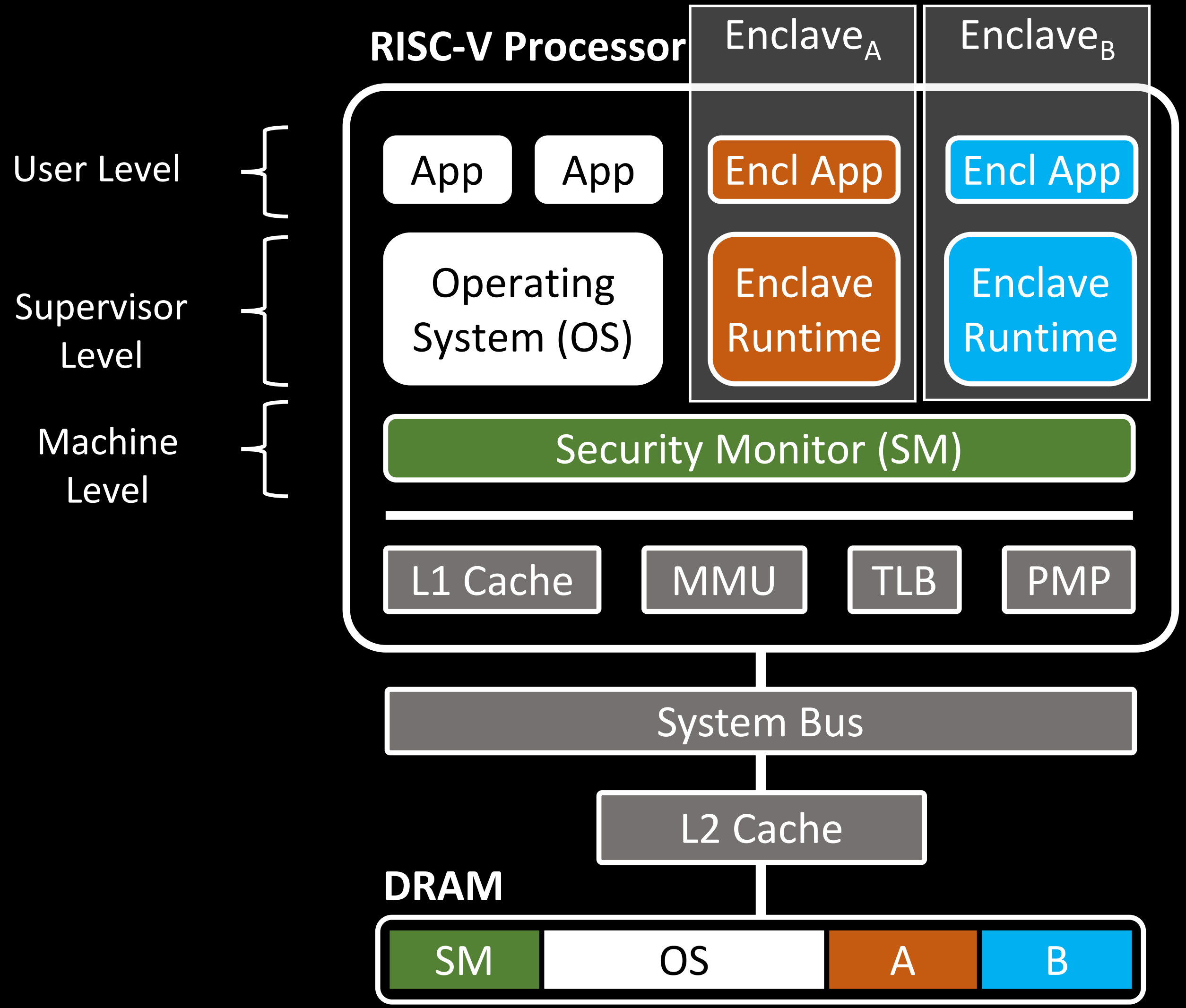

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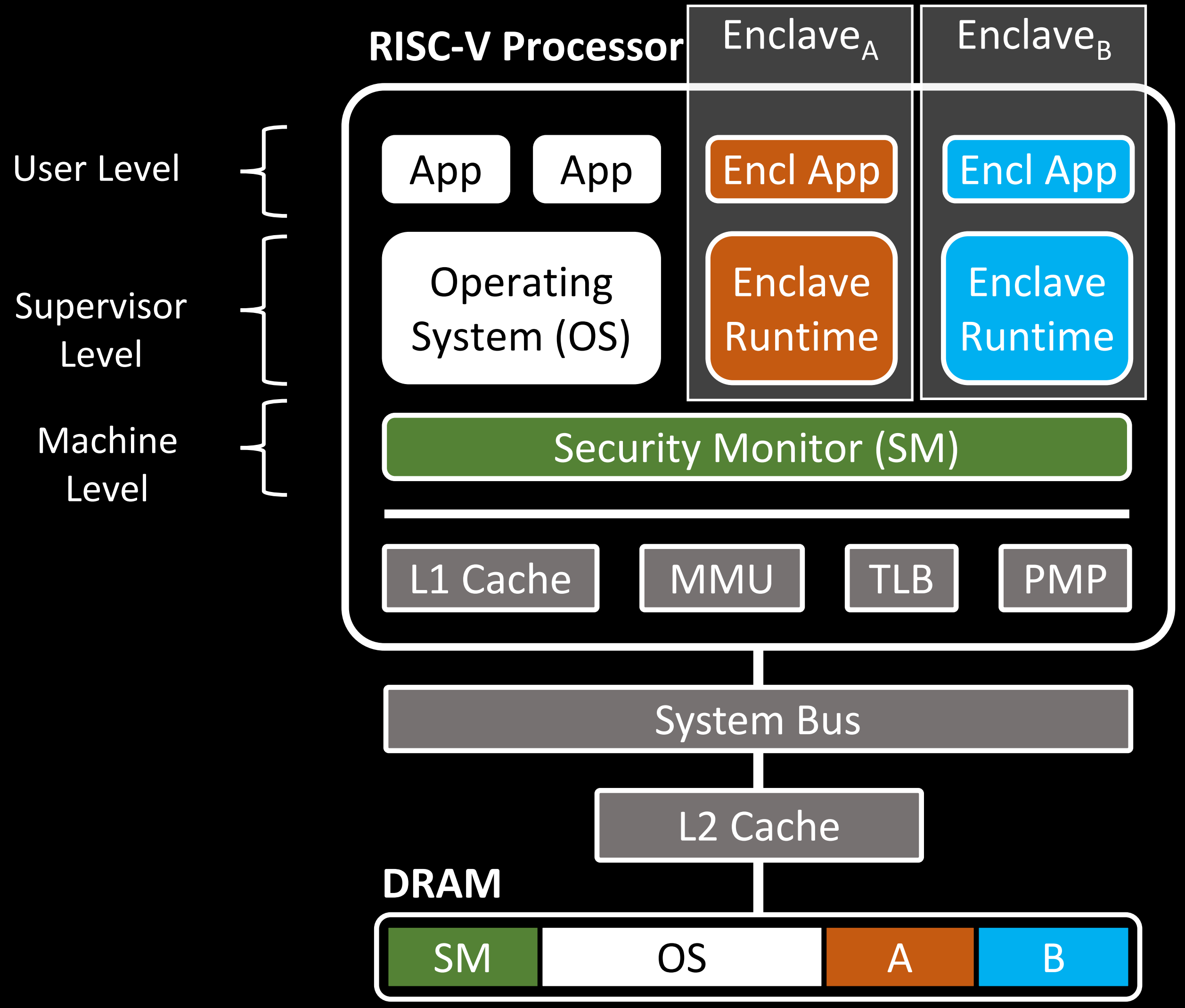

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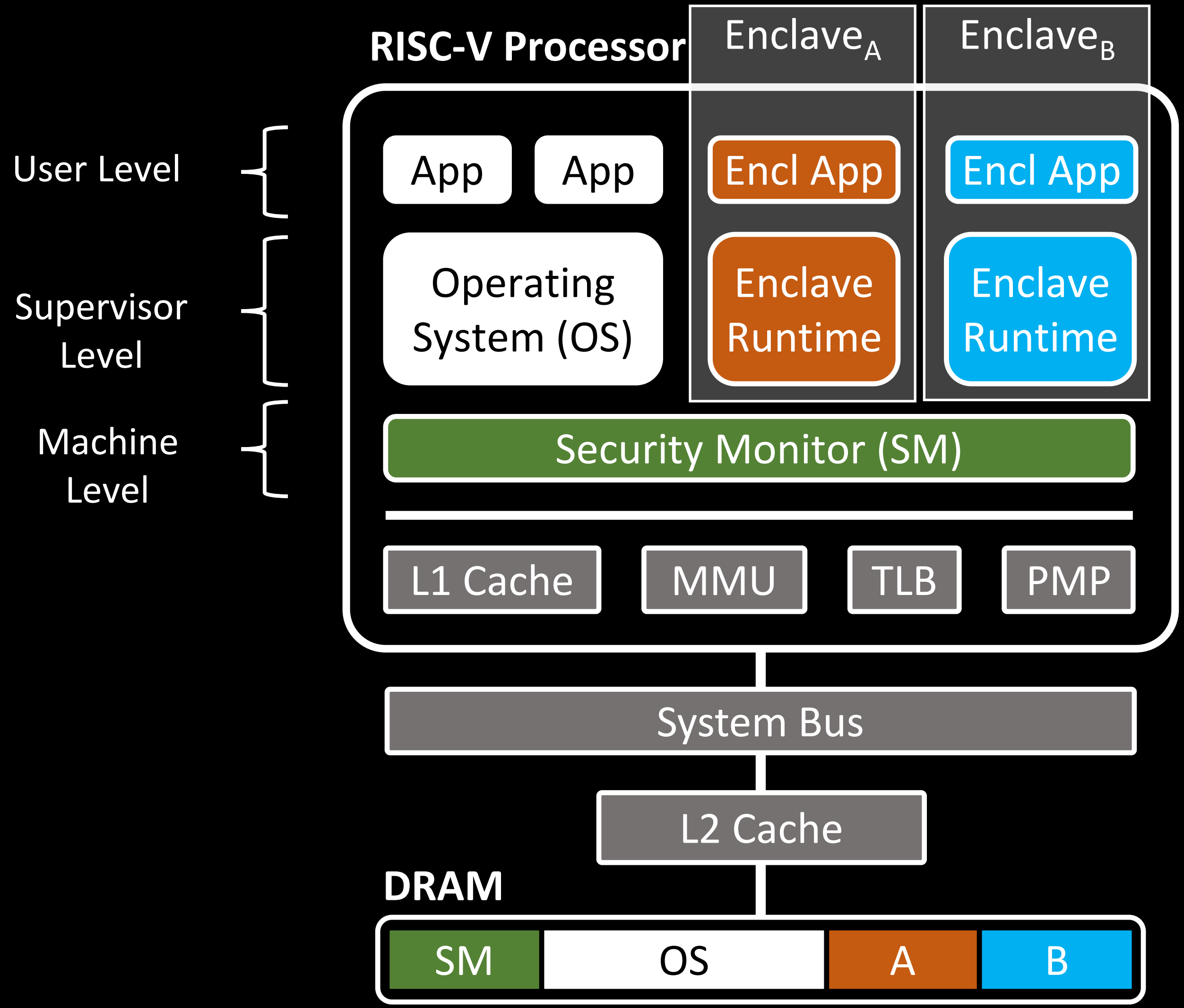

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- Assigns cache ways to processor cores

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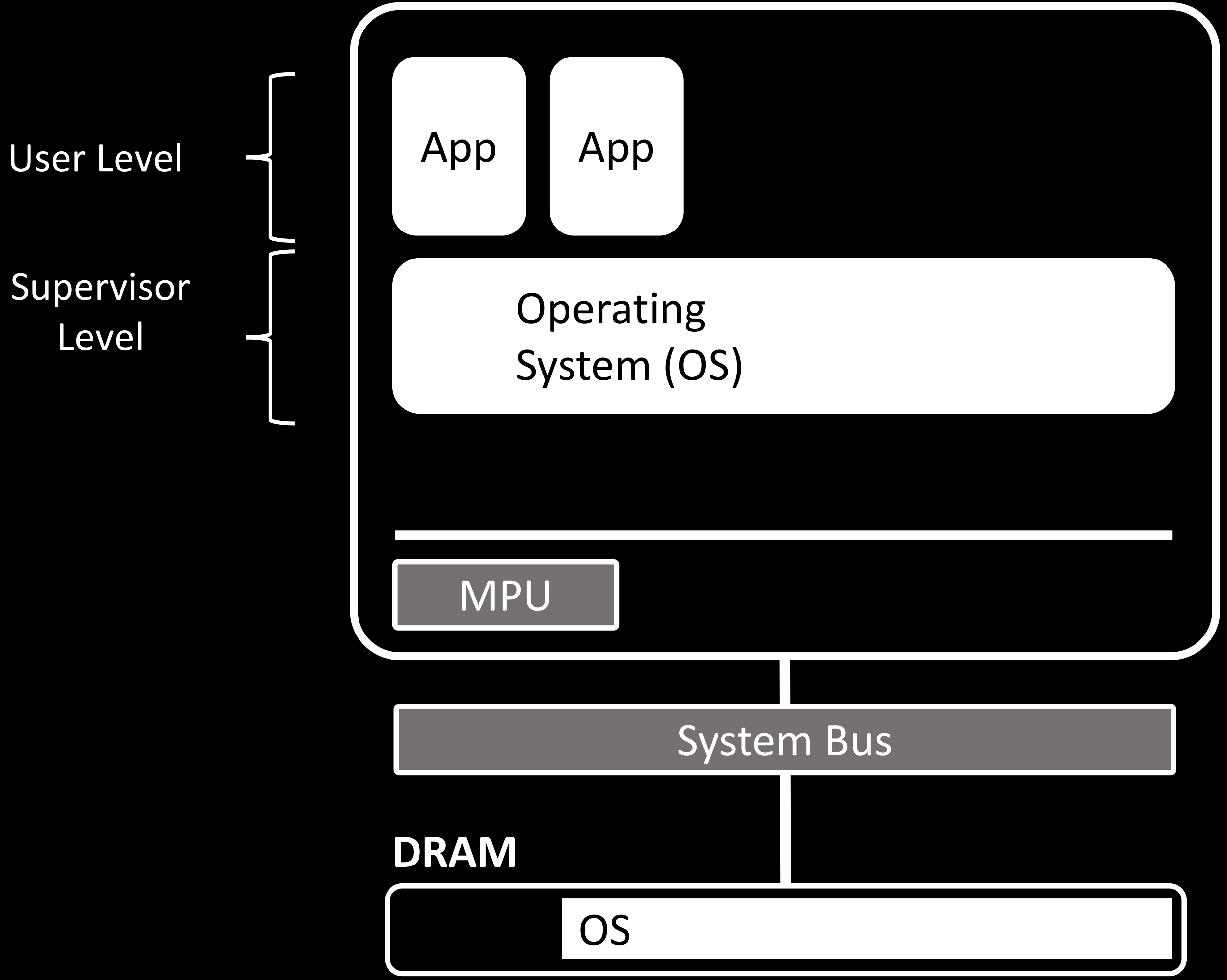
TIMBER-V



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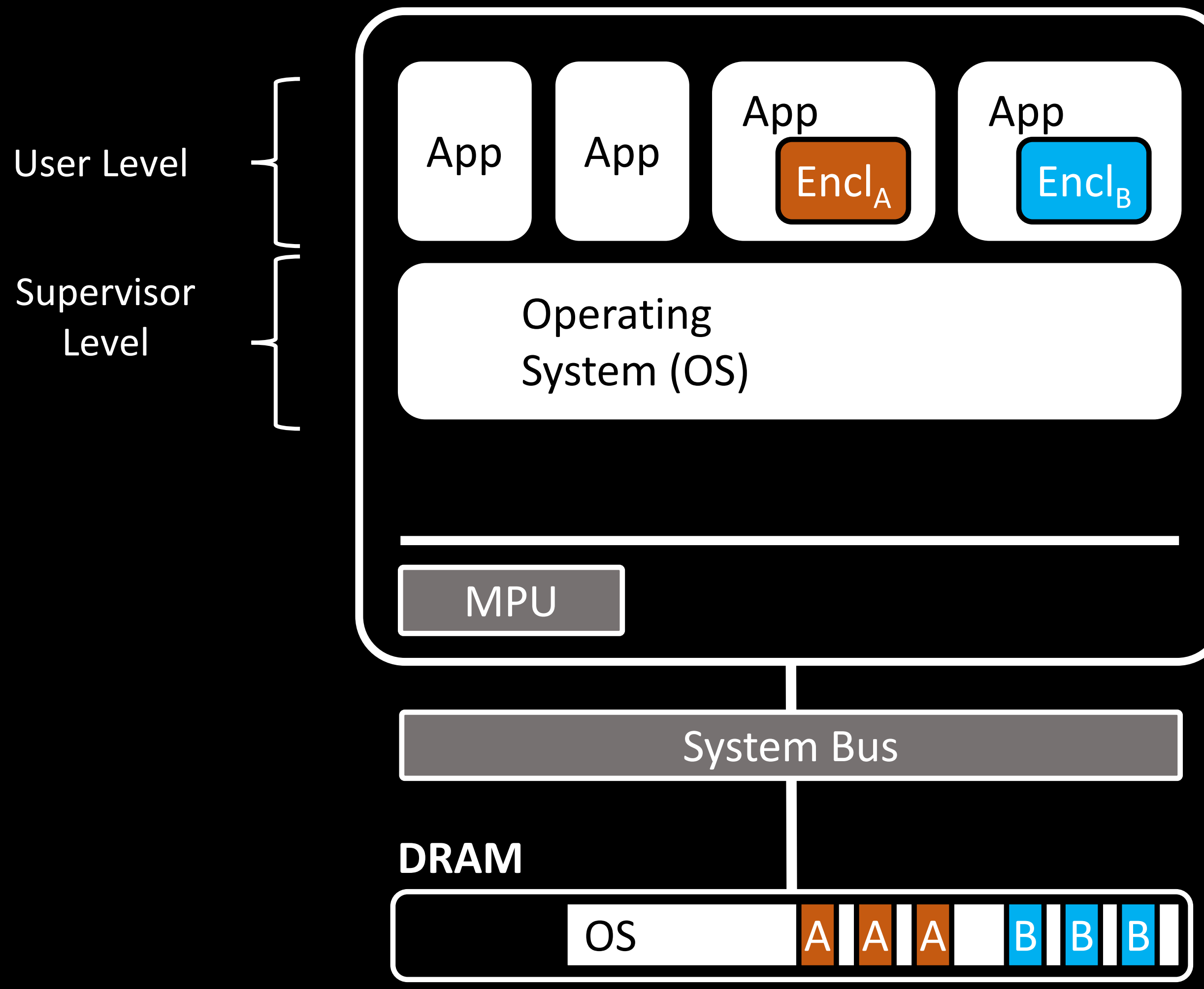

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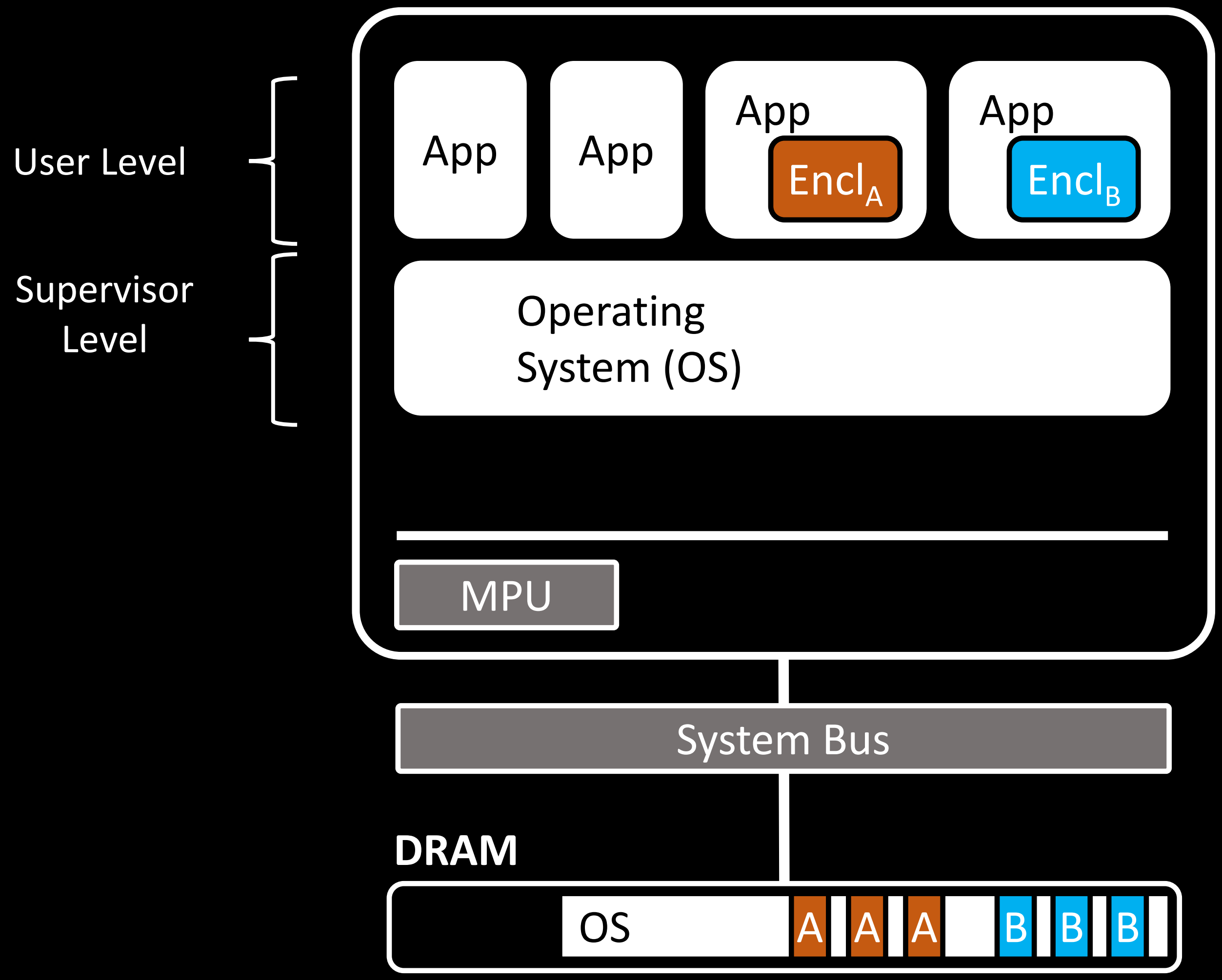

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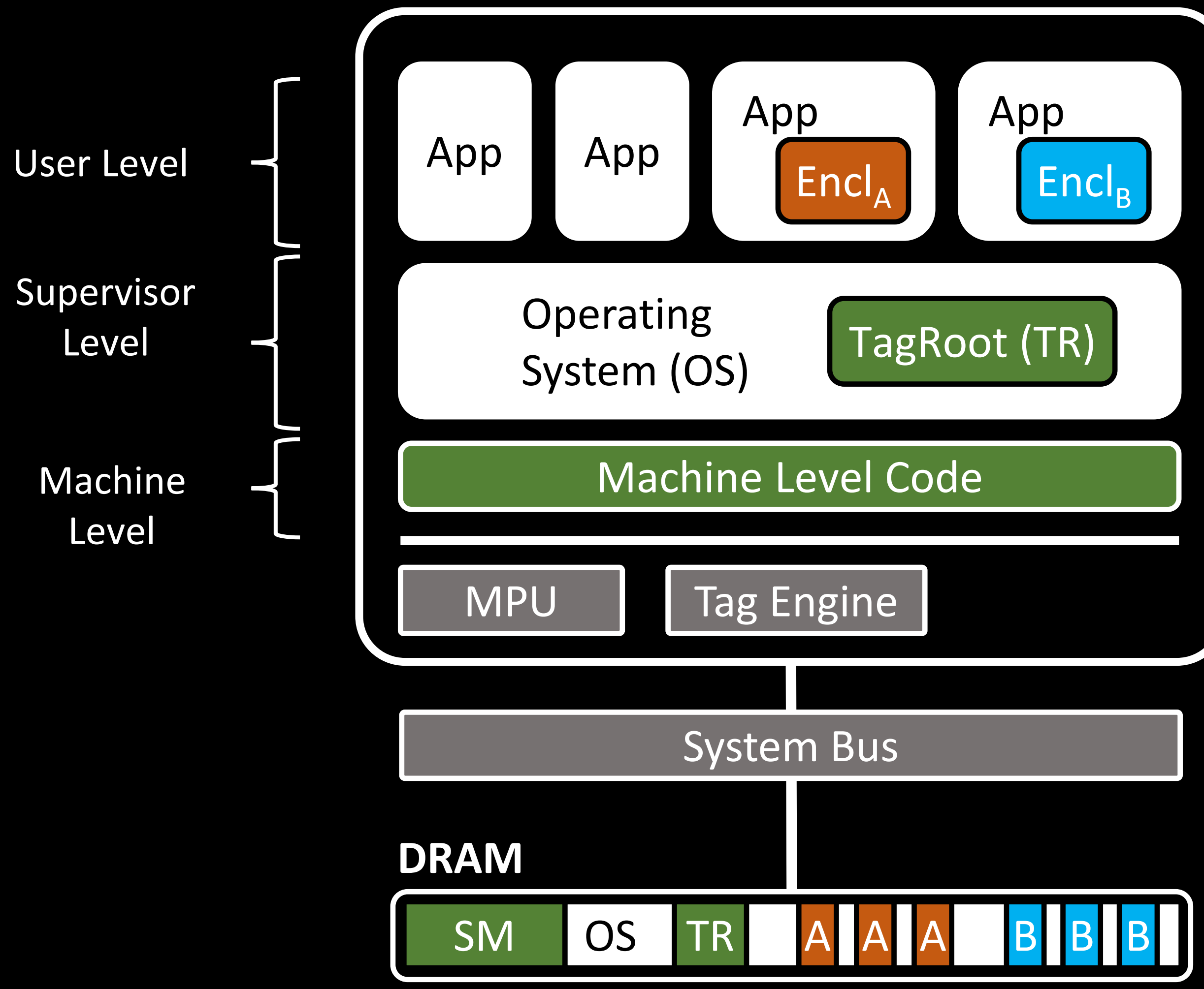

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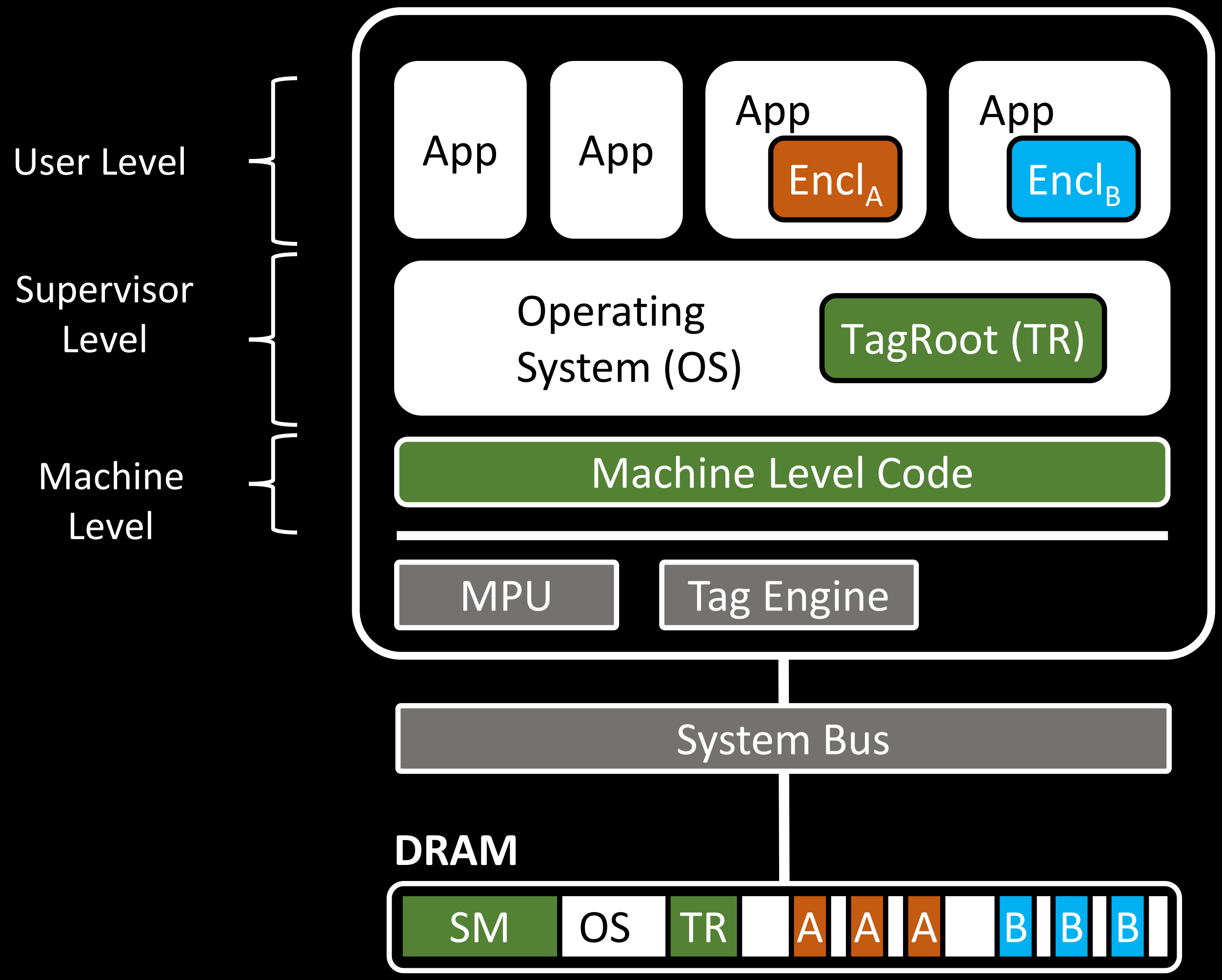

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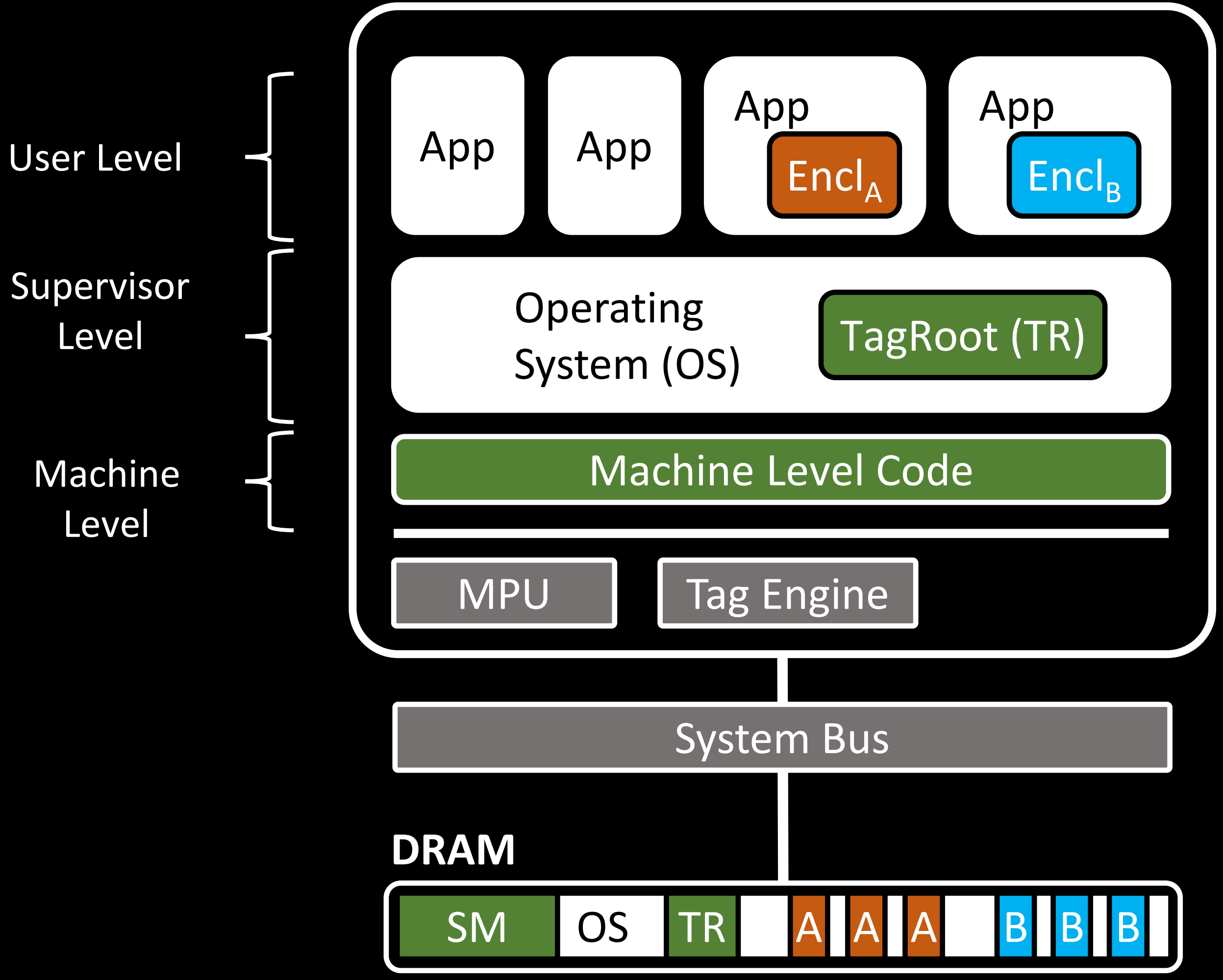

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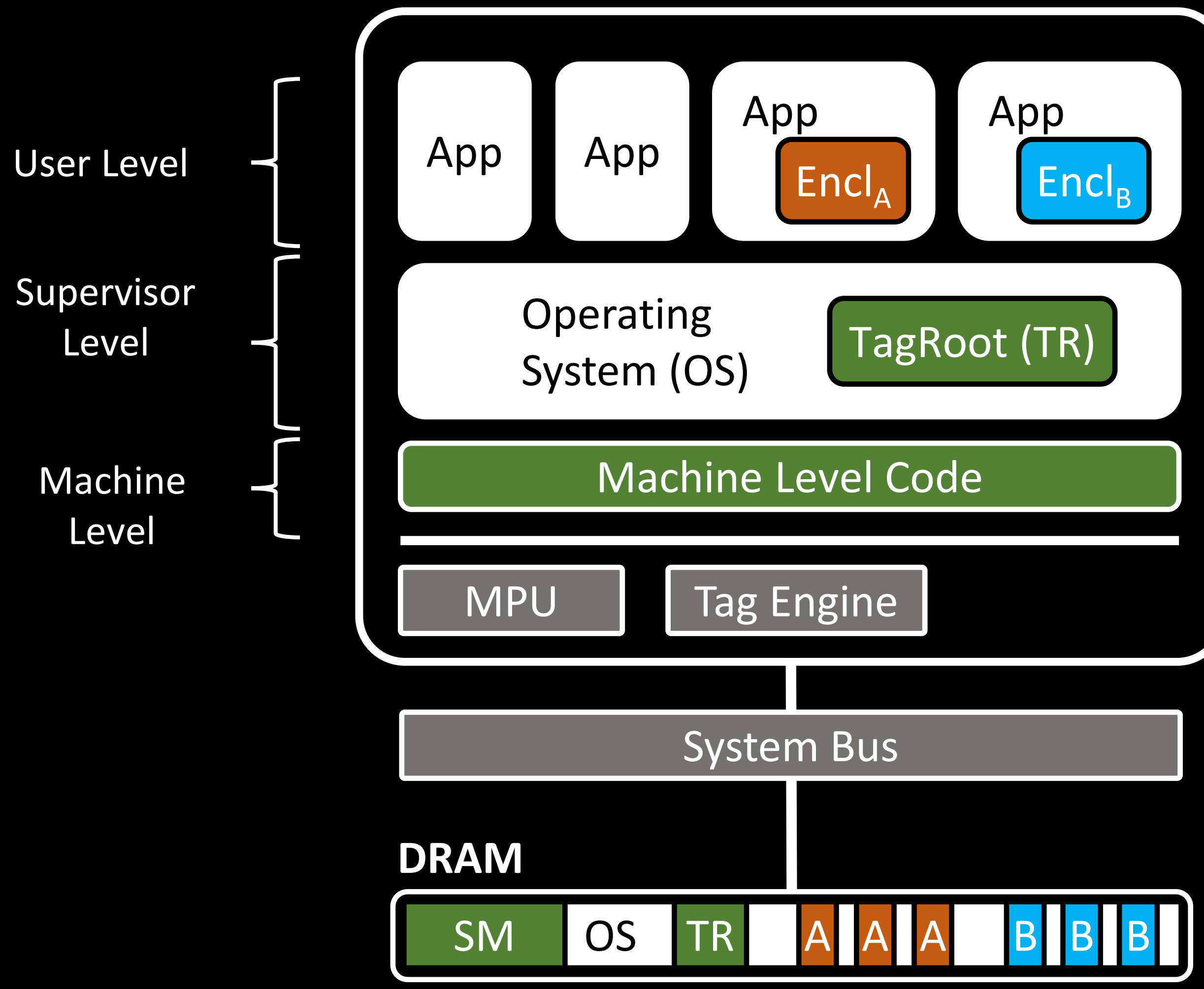

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- Cache memory not considered in the design

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Comparison RISC-V Enclave Security Architectures

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User level enclaves			
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Dynamic cache side-channel resilience			
Controlled side-channel resilience			
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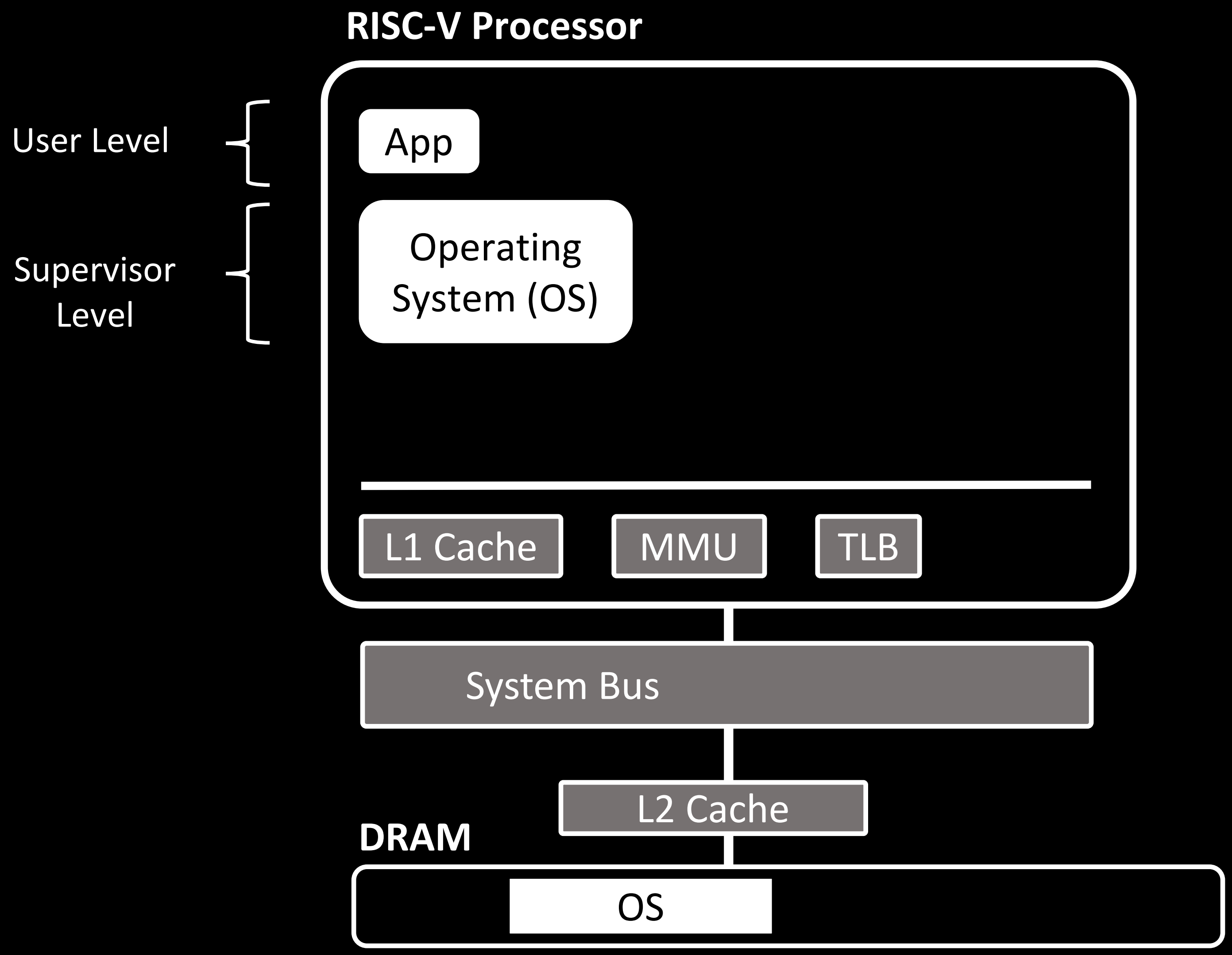

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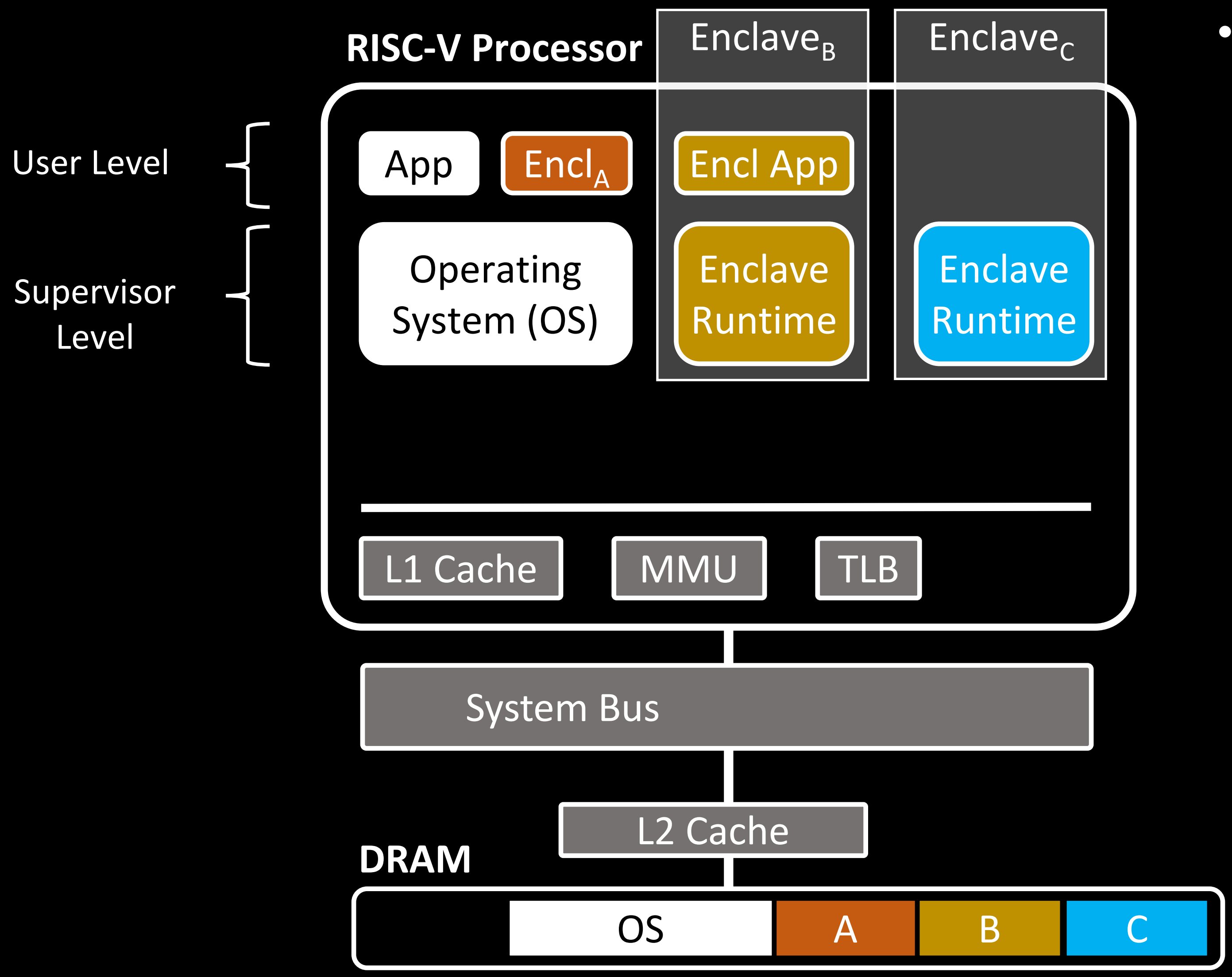

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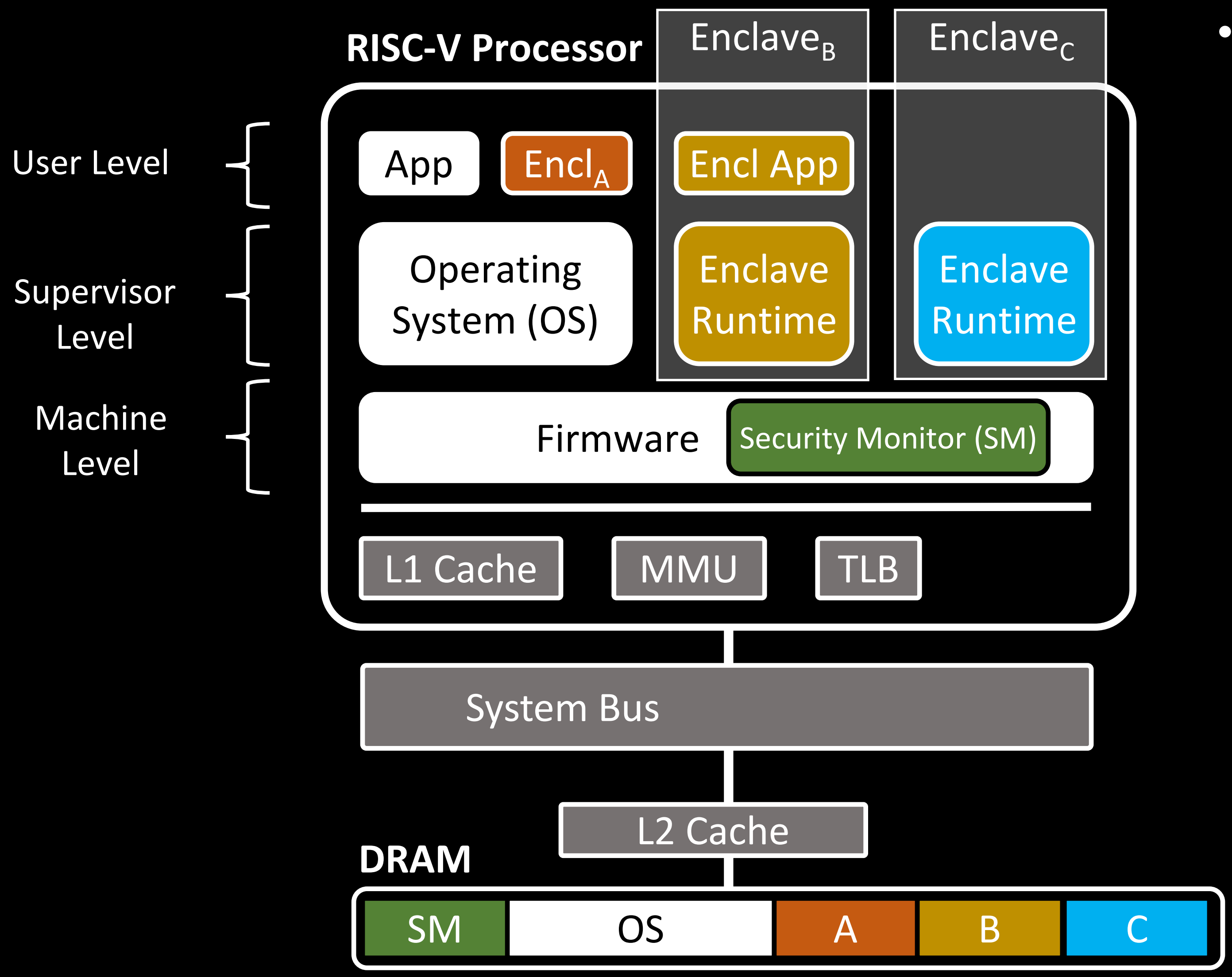

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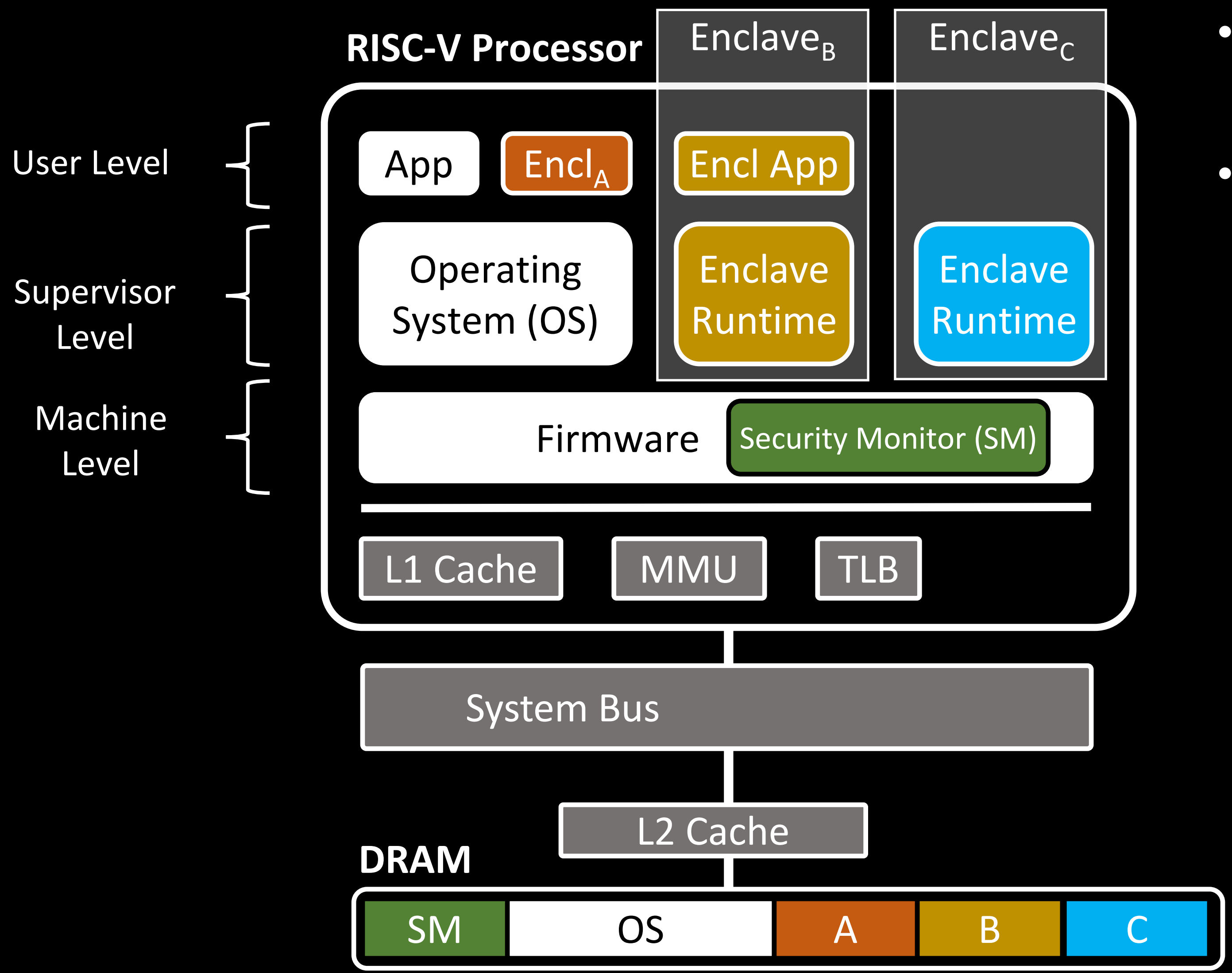

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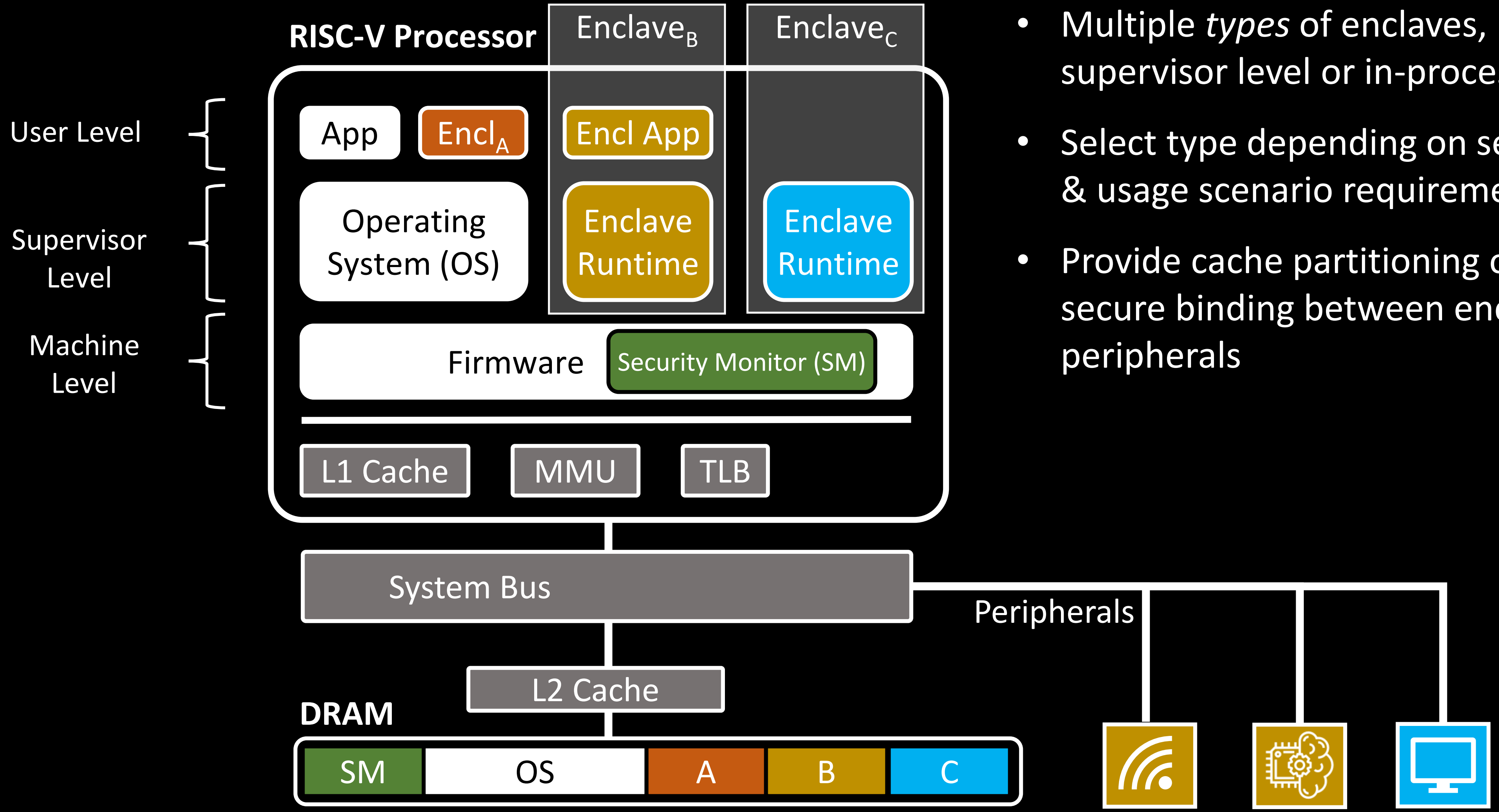

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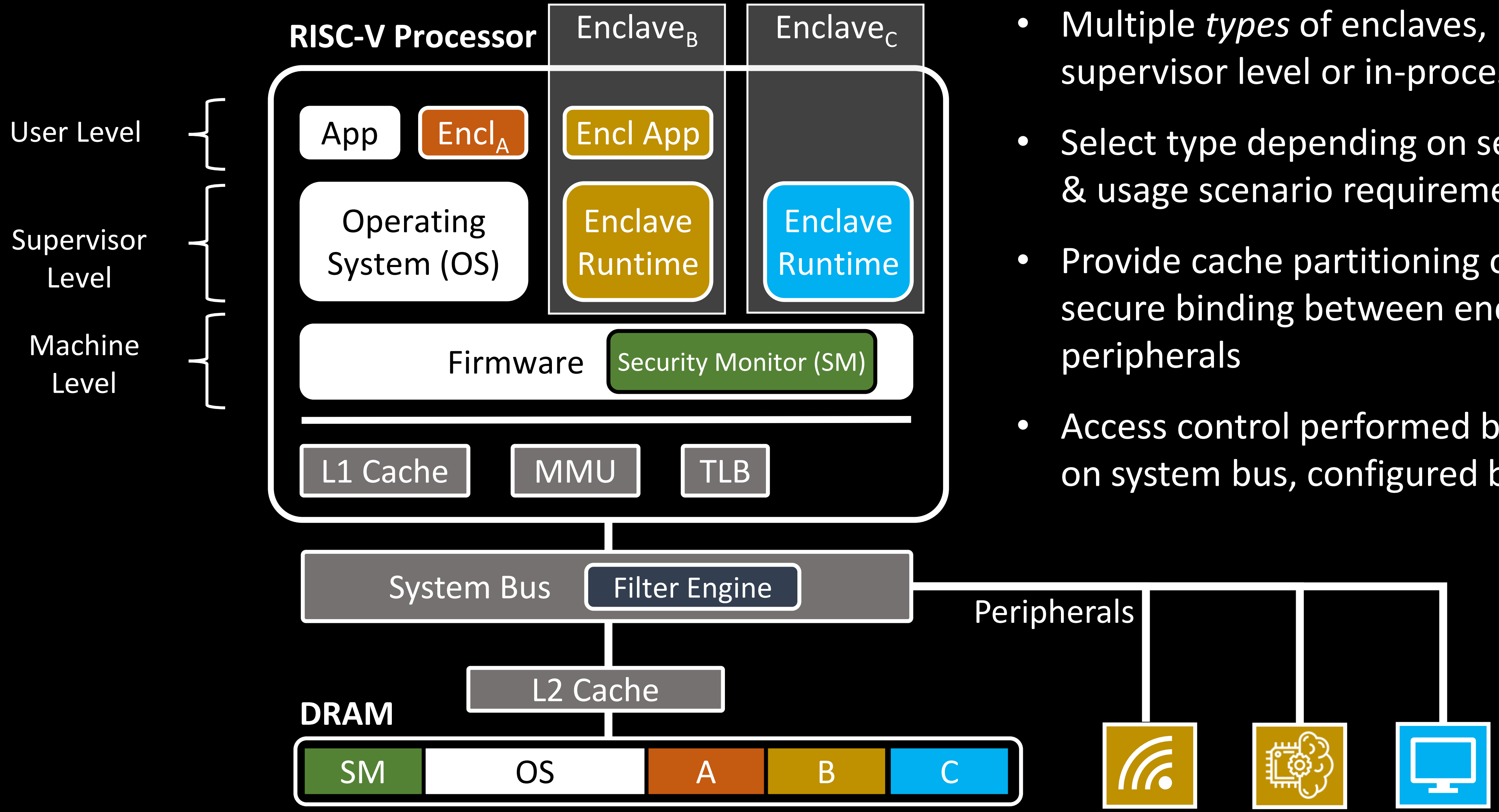

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  - Enclave architectures for Network-on-Chip platforms

Questions ?

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