STAM Center — SECURE, TRUSTED, AND ASSURED MICROELECTRONICS

ASU Ira A. Fulton Schools of Engineering — Arizona State University

CSE 520
Computer Architecture II

Structural, Data and Control Hazards

Prof. Michel A. Kinsy

1

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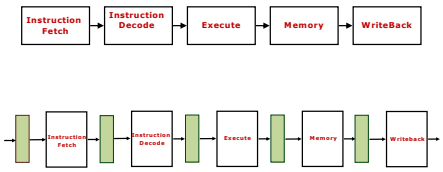
5-Stage RISC-V Pipelining



2

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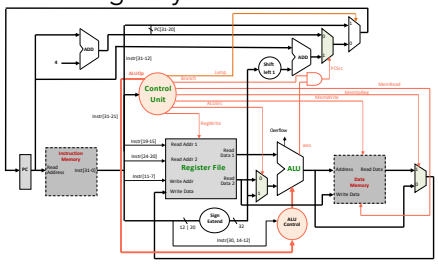
Single Cycle RISC-V CPU



3

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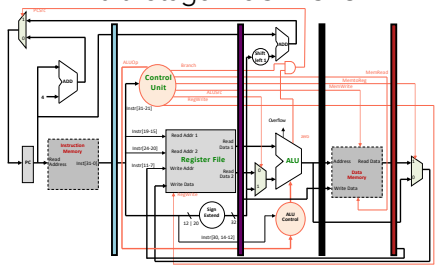
Multi-Stage RISC-V CPU



4

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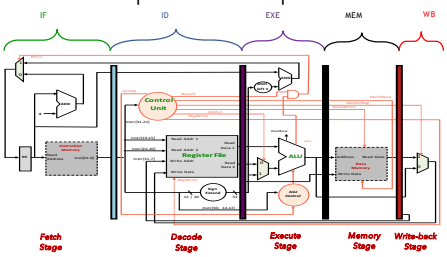
Pipelined Datapath



5

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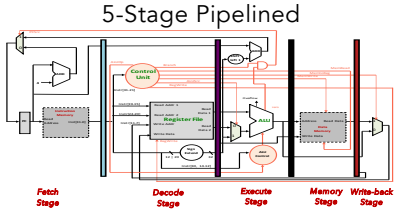
5-Stage Pipelined



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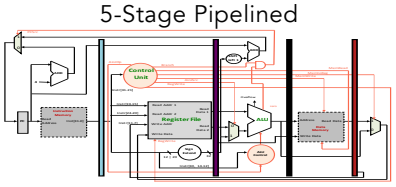
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF$_1$	ID$_1$							
Instruction2		IF$_2$							

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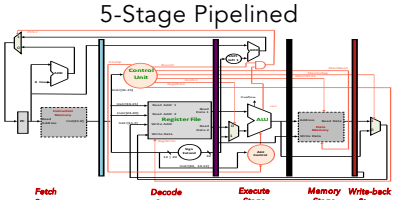
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF$_1$	ID$_1$	EX$_1$						
Instruction2		IF$_2$	ID$_2$						
Instruction3			IF$_3$						

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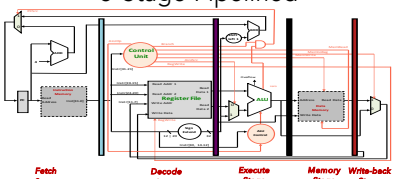
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF$_1$	ID$_1$	EX$_1$	MA$_1$					
Instruction2		IF$_2$	ID$_2$	EX$_2$					
Instruction3			IF$_3$	ID$_3$					
Instruction4				IF$_4$					

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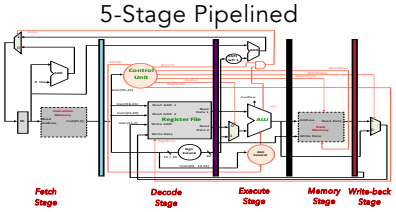
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
Instruction2		IF_2	ID_2	EX_2	MA_2				
Instruction3			IF_3	ID_3	EX_3				
Instruction4				IF_4	ID_4				
Instruction5					IF_5				

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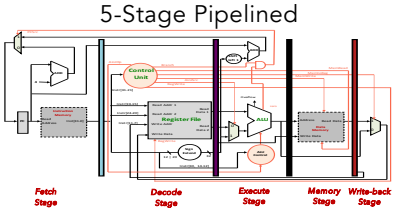
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
Instruction2		IF_2	ID_2	EX_2	MA_2	WB_2			
Instruction3			IF_3	ID_3	EX_3	MA_3			
Instruction4				IF_4	ID_4	EX_4			
Instruction5					IF_5	ID_5			

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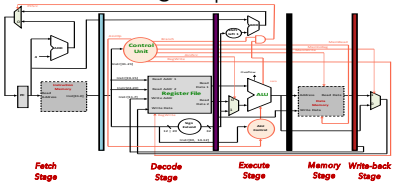
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
Instruction2		IF_2	ID_2	EX_2	MA_2	WB_2			
Instruction3			IF_3	ID_3	EX_3	MA_3	WB_3		
Instruction4				IF_4	ID_4	EX_4	MA_4		
Instruction5					IF_5	ID_5	EX_5		

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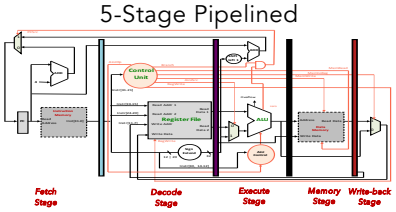
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
Instruction2		IF_2	ID_2	EX_2	MA_2	WB_2			
Instruction3			IF_3	ID_3	EX_3	MA_3	WB_3		
Instruction4				IF_4	ID_4	EX_4	MA_4	WB_4	
Instruction5					IF_5	ID_5	EX_5	MA_5	

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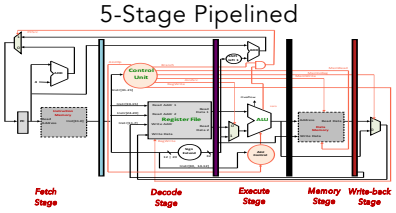
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
Instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
Instruction2		IF_2	ID_2	EX_2	MA_2	WB_2			
Instruction3			IF_3	ID_3	EX_3	MA_3	WB_3		
Instruction4				IF_4	ID_4	EX_4	MA_4	WB_4	
Instruction5					IF_5	ID_5	EX_5	MA_5	WB_5

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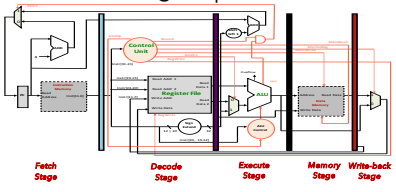
5-Stage Pipelined



Time	t0	t1	t2	t3	t4	t5	t6	t7	. . . .
instruction1	IF_1	ID_1	EX_1	MA_1	WB_1				
instruction2		IF_2	ID_2	EX_2	MA_2	WB_2			
instruction3			IF_3	ID_3	EX_3	MA_3	WB_3		
instruction4				IF_4	ID_4	EX_4	MA_4	WB_4	
instruction5					IF_5	ID_5	EX_5	MA_5	WB_5

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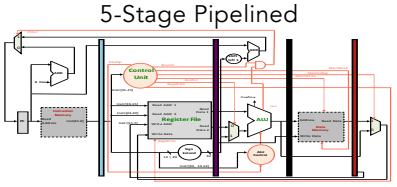
5-Stage Pipelined



Resources	time	t0	t1	t2	t3	t4	t5	t6	t7	. . .
	IF	I1	I2	I3	I4	I5				
	ID		I1	I2	I3	I4	I5			
	EX			I1	I2	I3	I4	I5		
	MA				I1	I2	I3	I4	I5	
	WB					I1	I2	I3	I4	I5

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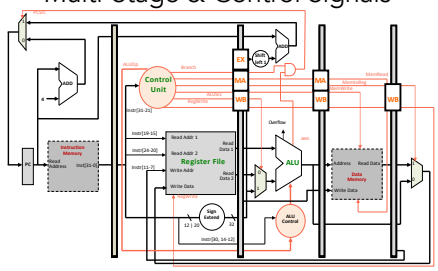
Multi-Stage & Control Signals



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Execution Simulation

- Consider the following instruction sequence

```
lw  x1, 8(x2)
sw  x3, 24(x4)
add x5, x6, x7
sub x8, x6, x7
lw  x1, 4(x2)
```

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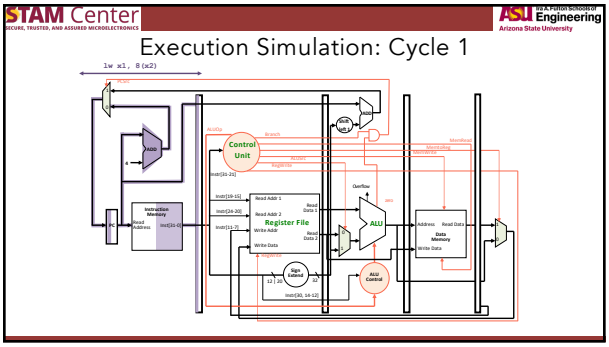
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Arizona State University
Execution Simulation: Cycle 1
lw x1, 8(x2)
Control Unit
Register File
ALU
Instruction Memory
Data Memory
ALU Control

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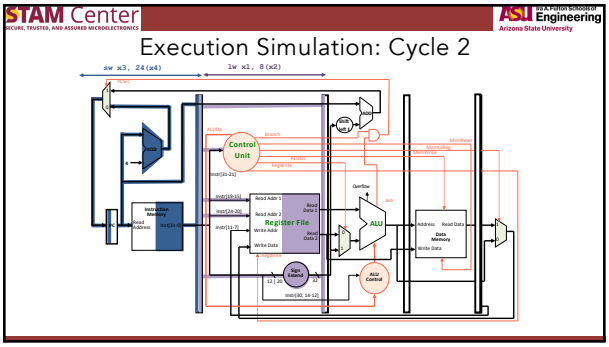
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Arizona State University
Execution Simulation: Cycle 2
sw x3, 24(x4)
lw x1, 8(x2)
Control Unit
Register File
ALU
Instruction Memory
Data Memory
ALU Control

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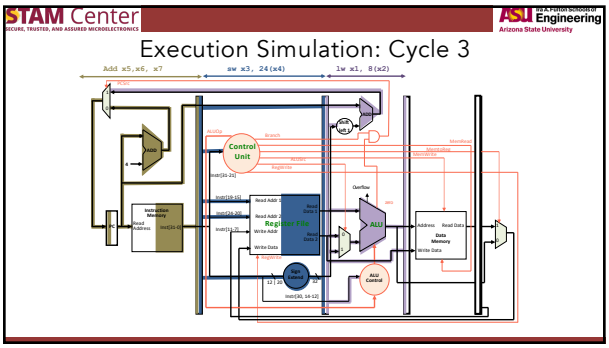
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Arizona State University
Execution Simulation: Cycle 3
Add x5,x6, x7
sw x3, 24(x4)
lw x1, 8(x2)
Control Unit
Register File
ALU
Instruction Memory
Data Memory
ALU Control

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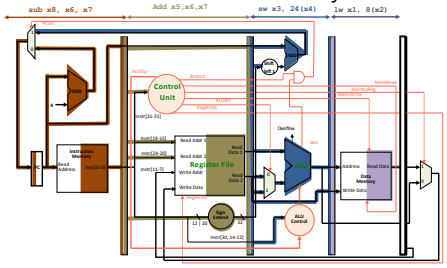
Execution Simulation: Cycle 4



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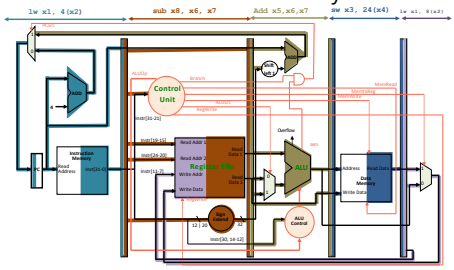
Execution Simulation: Cycle 5



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Instruction Interactions

- An instruction in the pipeline may need a resource being used by another instruction in the pipeline
  - Structural hazard
- An instruction may depend on something produced by an earlier instruction
  - Dependence may be for a data calculation
    - Data hazard
  - Dependence may be for calculating the next address
    - Control hazard (branches, interrupts)

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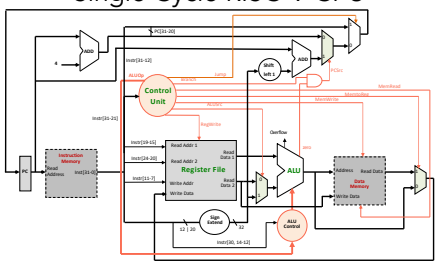
Single Cycle RISC-V CPU



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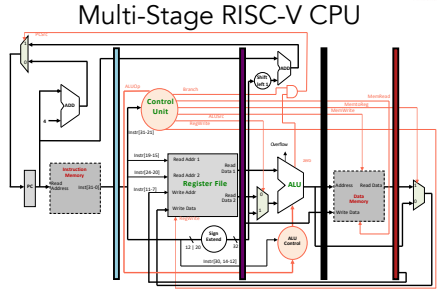
Multi-Stage RISC-V CPU



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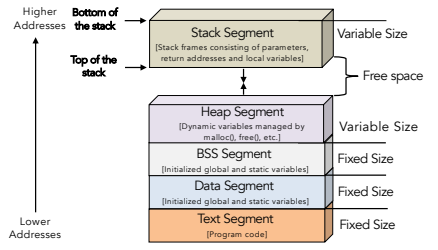
Program memory management



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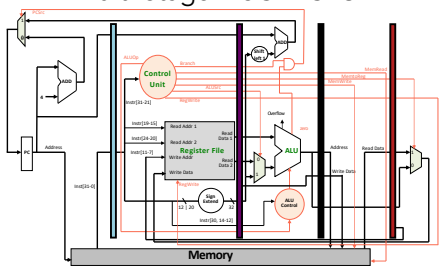
Multi-Stage RISC-V CPU



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Structural Hazard

- Consider the following instruction sequence

```
lw  x1, 8(x2)
sw  x3, 24(x4)
add x5, x6, x7
sub x8, x6, x7
lw  x1, 4(x2)
```

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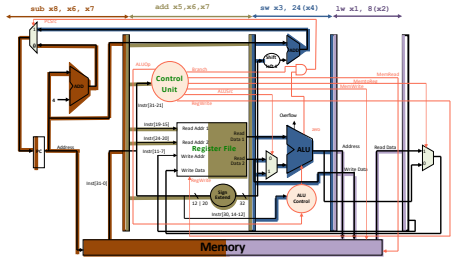
Structural Hazard



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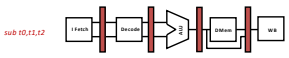
Instruction Interactions



sub t0,t1,t2
add t3,t4,t5
add t6,s2,s3
sub t1,s3,s2
lw t2,16(t4)
add t5,t5,s2
sw t0,16(s3)

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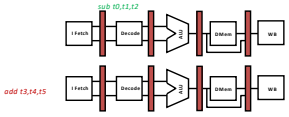
Instruction Interactions



sub t0,t1,t2
add t3,t4,t5
add t6,s2,s3
sub t1,s3,s2
lw t2,16(t4)
add t5,t5,s2
sw t0,16(s3)

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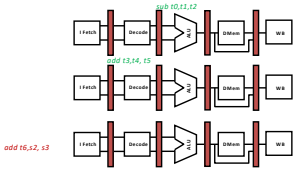
Instruction Interactions



sub t0,t1,t2
add t3,t4,t5
add t6,s2,s3
sub t1,s3,s2
lw t2,16(t4)
add t5,t5,s2
sw t0,16(s3)

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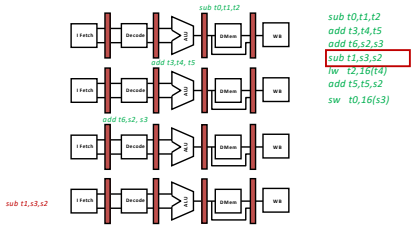
Instruction Interactions



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Instruction Interactions

- Supposed that we have the following set of instructions:

```
sub t0,t1,t2
add t3,t0,t4
add t5,t0,t6
sub s2,s3,t0
lw  s4,16(t0)
add s4,s4,s2
sw  s4,16(t0)
```

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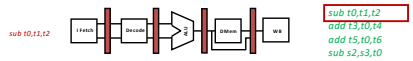
Instruction Interactions




```
sub t0,t1,t2
add t3,t0,t4
add t5,t0,t6
sub s2,s3,t0
lw  s4,16(t0)
add s4,s4,t7
sw  s4,16(t0)
```

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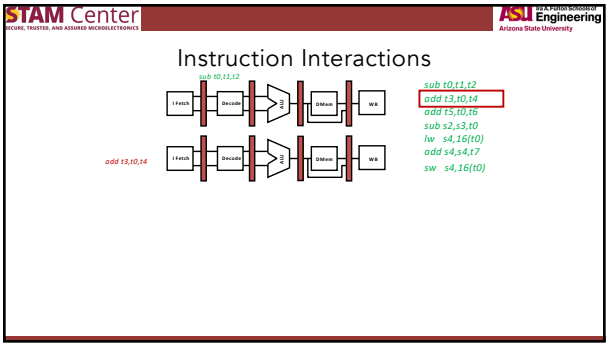
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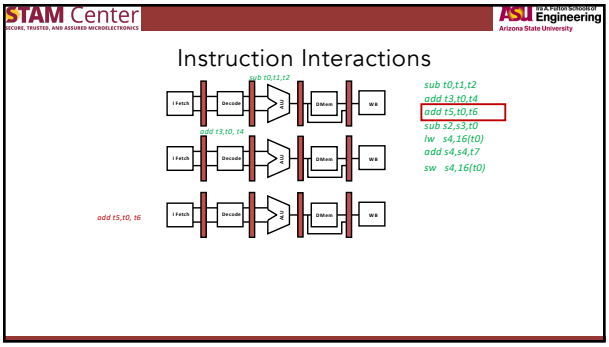
SECURE, TRUSTED, AND ASSURED MICROELECTRONICS
ASU Ira A. Fulton Schools of Engineering
Arizona State University
Instruction Interactions
sub t0,t1,t2
add t3,t0,t4
I Fetch
Decode
EX
DMem
WB
sub t0,t1,t2
add t3,t0,t4
add t5,t0,t6
sub s2,s3,t0
lw s4,16(t0)
add s4,s4,t7
sw s4,16(t0)

37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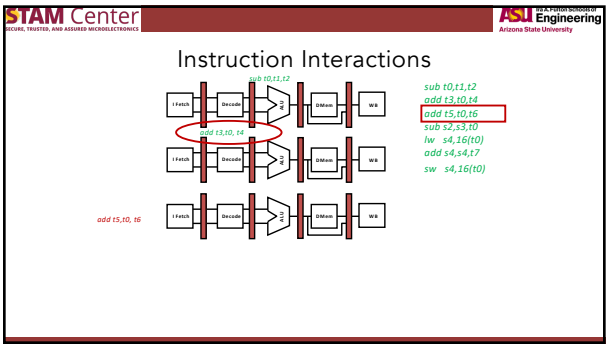
add t5,t0,t6
sub s2,s3,t0
lw s4,16(t0)
add s4,s4,t7
sw s4,16(t0)

38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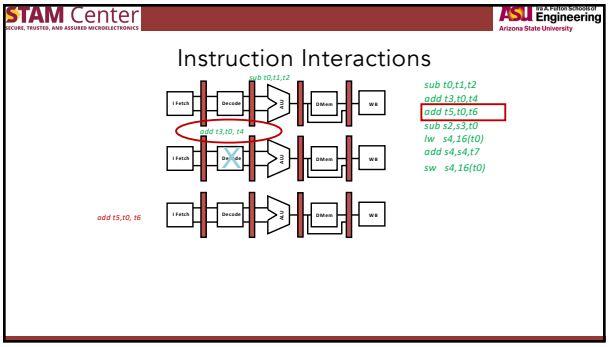
lw s4,16(t0)
add s4,s4,t7
sw s4,16(t0)

39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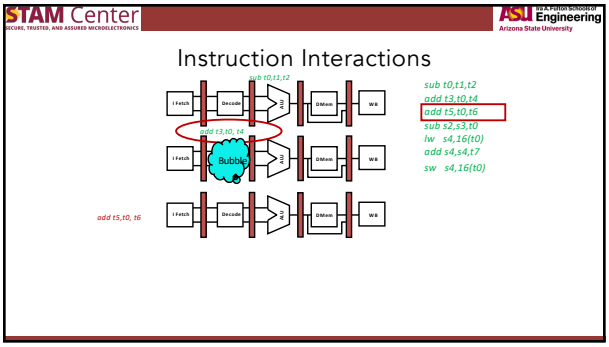
add s4,s4,t7
sw s4,16(t0)
I Fetch
Decode
EX
DMem
WB
add t5,t0, t6

40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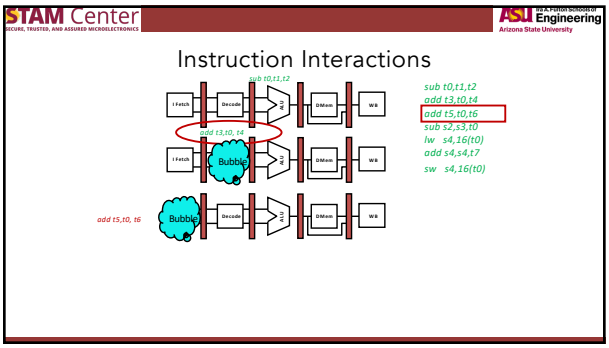
add s4,s4,t7
sw s4,16(t0)
I Fetch
Decode
EX
DMem
WB
Bubble
add t5,t0, t6

41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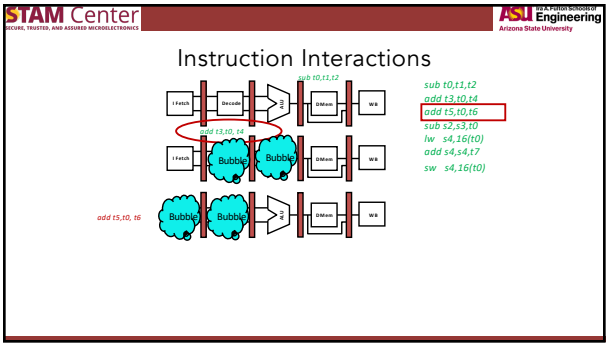
add s4,s4,t7
sw s4,16(t0)
I Fetch
Decode
EX
DMem
WB
Bubble
Bubble
add t5,t0, t6

42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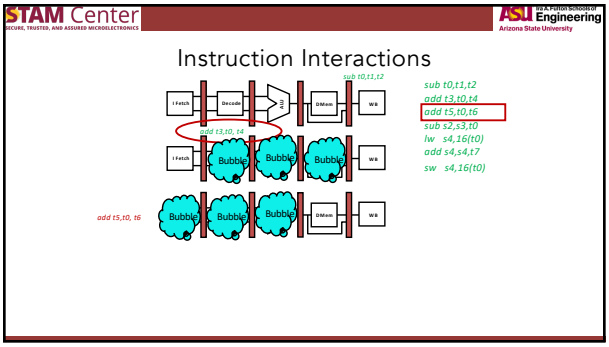
sw s4,16(t0)
I Fetch
Decode
EX
DMem
WB
Bubble
add t5,t0, t6

43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add s4,s4,t7
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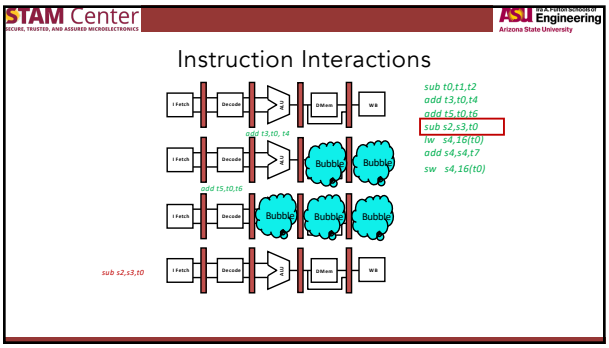
I Fetch
Decode
EX
DMem
WB
Bubble
add t5,t0, t6

44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add t5,t0,t6
sub s2,s3,t0
lw s4,16(t0)
add s4,s4,t7
sw s4,16(t0)
I Fetch
Decode
EX
DMem
WB
Bubble
sub s2,s3,t0

45

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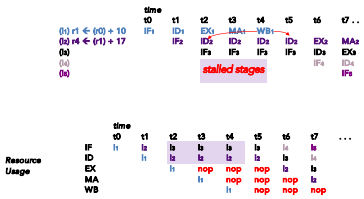
Stalled Stages and Pipeline



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Stalled Stages and Pipeline

- Pipelining was introduced to improve performance

$$\frac{\text{Time}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} * \frac{\text{Cycles}}{\text{Instruction}} * \frac{\text{Time}}{\text{Cycle}}$$

- But with stalling, CPI will go up
- So we need a way to reduce stalling cycles!

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Next Learning Module

- CPU: Hazard Resolution

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