CSE 520
Computer Architecture II

On-Chip Networking

Prof. Michel A. Kinsy

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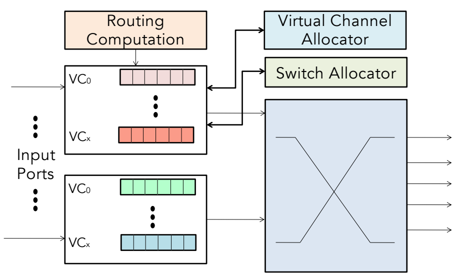
Virtual Channel Router



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What's In A Router?

- It's a system as well
  - Logic – State machines, Arbiters, Allocators
    - Control the movement through router
    - Idle, Routing, Waiting for resources, Active
  - Memory – Buffers
    - Store flits before forwarding them
    - SRAMs, registers, processor memory
  - Communication – Switches
    - Transfer flits from input to output ports
    - Crossbars, multiple crossbars, fully-connected, bus

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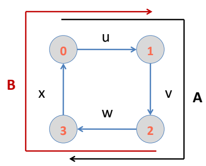
Network Deadlock

- Flow A holds u and v but cannot make progress until it acquires channel w
- Flow B holds channels w and x but cannot make progress until it acquires channel u



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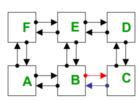
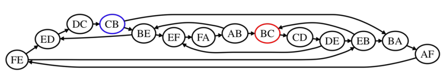
Channel Dependency Graph

- Can create a channel dependency graph (CDG) of the network

Vertices in the C DG represent net work *links*



Disallowing 180° turns, e.g., AB → BA



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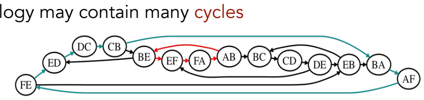
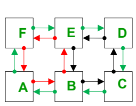
Cycles in CDGs

- The channel dependency graph D derived from the network topology may contain many cycles





Flow routed through links AB, BE, EF
Flow routed through links EF, FA, AB
Deadlock!

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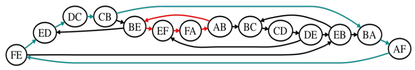
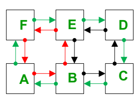
Key Insight

- If routes of flows conform to acyclic CDG, then there will be no possibility of deadlock!





Disallow/Delete certain edges in CDG

Edges in CDG correspond to turns in network!

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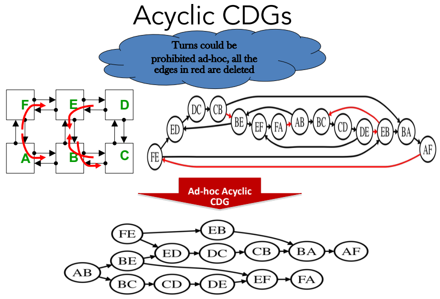
Acyclic CDGs



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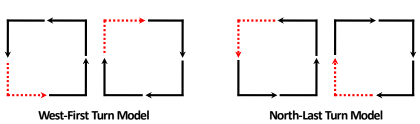
Turn Model (Glass and Ni, 1994)

- A systematic way of generating deadlock-free routes with small number of prohibited turns
- Deadlock-free if routes conform to at least ONE of the turn models (acyclic channel dependence graph)



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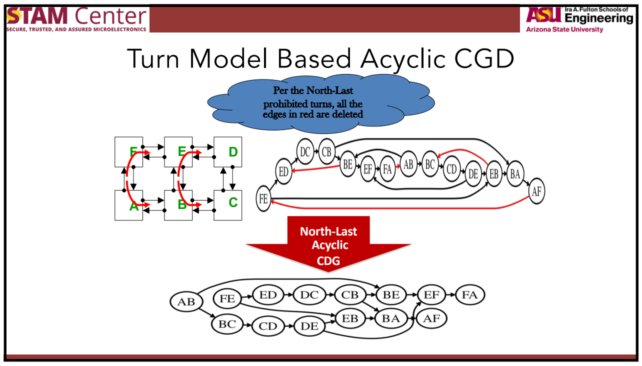
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Turn Model Based Acyclic CGD
Per the North-Last prohibited turns, all the edges in red are deleted
F
E
D
A
B
C
North-Last Acyclic CDG
AB
FE
ED
DC
CB
BE
EF
FA
BC
CD
DE
EB
BA
AF

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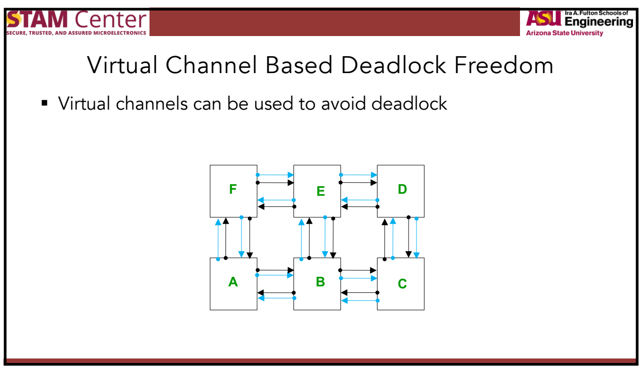
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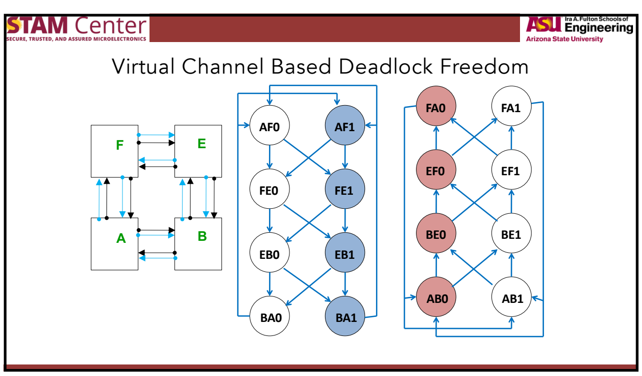
Virtual Channel Based Deadlock Freedom
Virtual channels can be used to avoid deadlock
F
E
D
A
B
C

11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Virtual Channel Based Deadlock Freedom
F
E
A
B
AF0
AF1
FE0
FE1
EB0
EB1
BA0
BA1
FA0
FA1
EF0
EF1
BE0
BE1
AB0
AB1

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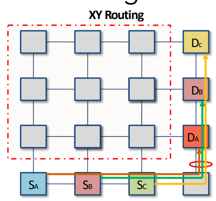
On-Chip Network Routing

- Oblivious Routing
- Statically determined given the source and destination addresses
  - (+) Simple and fast router designs
  - (-) Lead to network under-utilization
  - (-) Lack proper load balancing



Link Capacity 75 Mbytes/sec
Each flow has 25 Mbytes/sec bandwidth demand

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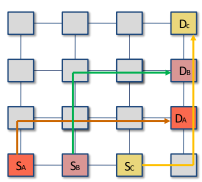
Adaptive Routing

- Routes dynamically adjusted based on network status
  - (+) Better load balancing and path diversity
  - (+) Potentially better throughput and latency
  - (-) Need for global or local knowledge of network conditions
  - (-) Router complexity



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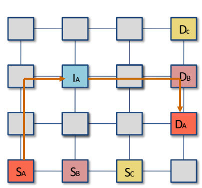
Valiant's Routing Algorithm

- Randomized Routing
  - A packet, going from node SA to node DA, is first routed from SA to a randomly chosen intermediate node IA, before going from IA to final destination DA.
  - It helps load-balance the network and has a good worst-case performance at the expense of locality



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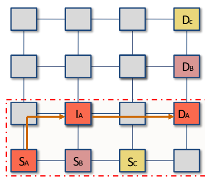
ROMM Routing

- ROMM: Randomized, Oblivious Multi-phase Minimal Routing
  - In an effort to retain locality in routing of packets, the intermediate node is confined to a minimal quadrant
  - This approach essentially translates into randomly selecting between the various minimal paths from the source to the destination



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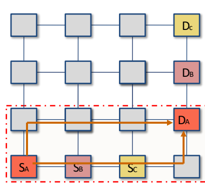
O1TURN Routing

- Orthogonal One-Turn Routing
  - O1TURN: Restricted version of ROMM routing where the intermediate node is one of the corners of the minimum quadrant
  - O1TURN allows each packet to traverse one of at most two routes with equal probability



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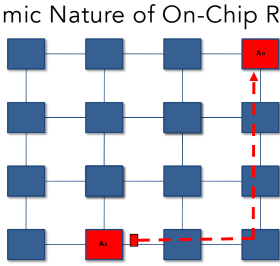
Dynamic Nature of On-Chip Routing



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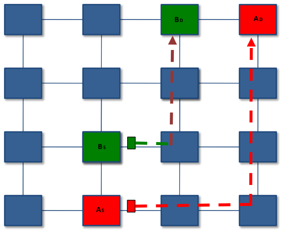
Dynamic Nature of On-Chip Routing



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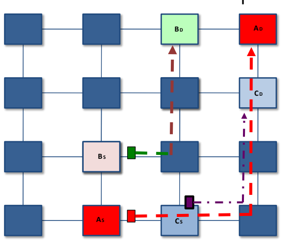
Dynamic Nature of On-Chip Routing



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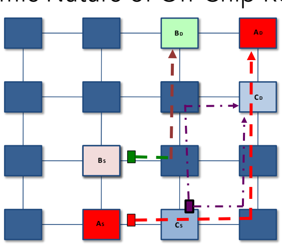
Dynamic Nature of On-Chip Routing



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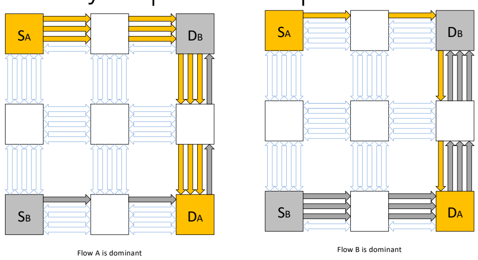
Polymorphic On-Chip Network



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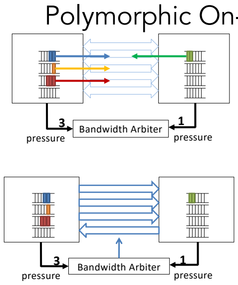
Polymorphic On-Chip Network



- The ability to sense
- And self-modify

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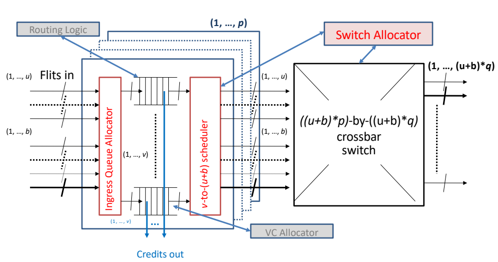

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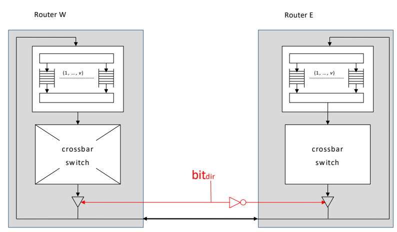

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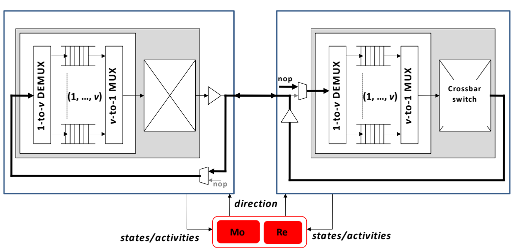

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Next Learning Module

- Advanced Architectures
  - AI Architectures

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