STAM Center
SECURE, TRUSTED, AND ASSURED MICROELECTRONICS

Ira A. Fulton Schools of Engineering
Arizona State University

CSE 520 Computer Architecture II
Term: Spring 2026
Lead Instructor: **Prof. Michel A. Kinsy**

Self-Assessment

Assigned Jan. 12th, 2026 ***Due Jan. 14, 2026***

http://ascslab.org/courses/cse520/index.html

This problem set is intended as an assessment to determine your background. For each question, we ask that you fill out the table at the end of the problem set handout indicating your level of confidence with each assigned problem and hand this in with your solutions. If you have never seen the material before, then please enter "0". If you have seen the material, and think you should know it, but can't answer the question without spending time studying your old notes, then please enter "1". If you are comfortable with the material, then enter "2". You should turn in solutions for problems where you entered "1" and "2", but do not have to turn in solutions for problems for which you entered a "0".

If there are too many "0"s in the table then it is unlikely you will be able to keep up with CSE 520 this term, as the pace is such that you will not be able to take prerequisite material concurrently. If you are not sure whether you have the background to take this class, please feel free to discuss your particular situation with the instructor.

You must work individually and turn in your own solutions. Do not discuss the problems with others.

Name:

Problem 1

A) C Program analysis

```
void foo(int *i){
    *i = *i + 1;
}

void main(void){
    int array [] = { 10, 20, 30, 40, 50 };
    int i, *ptr ;
    ptr = array;
    for ( i = 0 ; i <4 ; i++ ){
        foo(ptr++);
        printf ("\n%", *ptr ) ;
    }
}
```

What will be the output of the following program?

i) 11 21 31 41
ii) 20 30 40 50
iii) 21 31 41 51
iv) 10 20 30 40

B) C Program key semantics

```
#define MAX_NUM 15
```

Referring to the sample above, what is *MAX_NUM*?
i) MAX_NUM is a precompiler constant
ii) MAX_NUM is a preprocessor macro
iii) MAX_NUM is an integer variable
iv) MAX_NUM is a linker constant

Problem 2

The number 1.248 is equal to 1 + 2/10 + 4/100 + 8/1000. If we use a binary point instead of a decimal point, what will the following numbers equal to in Base-10 and Base 16?

A) 0.101
B) 1.001
C) 00.101
D) 11.101
E) 1010.101

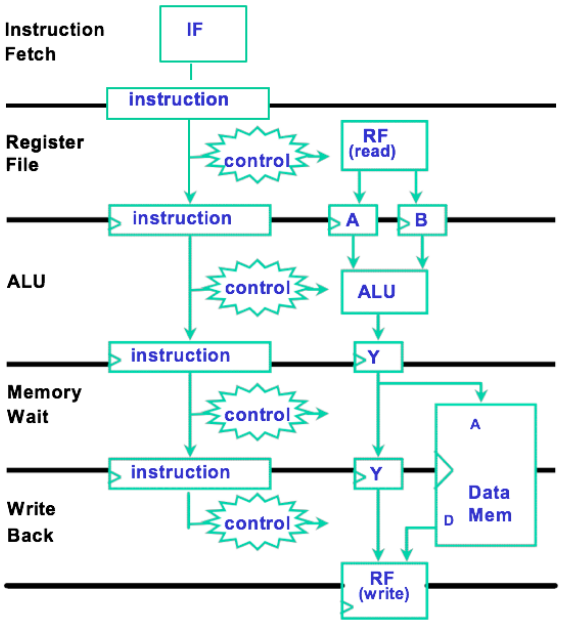
Problem 3

A) Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor. Name any intermediate representations that the code may take.
B) What is the difference between stack and heap?
C) What happens if the stack and heap segments collide (i.e., one overwrites part of the other)? Why is this dangerous? How would you prevent it?
D) What are the causes a stack overflow? Give a specific example.
E) What is the difference between the .BSS and .DATA segments

Problem 4

The following figure shows a 5-stage pipelined processor. The pipelined processor should always compute the same results as an unpipelined processor. Answer the following questions for each of the instruction sequences below:

- Why does the sequence require special handling (what could go wrong)?
- What are the minimal hardware mechanisms required to ensure correct behavior?
- What additional hardware mechanisms, if any, could help preserve performance? Assume that the architecture does not have any branch delay slots, and assume that branch conditions are computed by the ALU.




```
A)  BEQ     r1, r0, 200     # branch to PC+200 if r1 == r0
    ADD     r2, r3, r5      # r2 ← r3 + r5
    SUB     r4, r5, r6      # r4 ← r5 + r6
    …
B)  ADD     r1, r0, r2      # r1 ← r0 + r2
    SUB     r4, r1, r2      # r4 ← r1 - r2
    …
C)  LD      r1, 0(r2)       # r1 ←Mem[r2+0] ADD
            r3, r1, r2      # r3 ← r1 + r2
    …
```

Problem 5

A) With a 32-bit address, how many total **Tag** bits are required for a direct-mapped cache with 256 bytes of data and 16-byte blocks?

B) Give the block number to map byte address **0x0018** to, when we have a 16-block direct-mapped cache, with 16-byte blocks and Tag bits are the high order bits.

C) Suppose we have a 2-Way Set Associative cache with 256 bytes of data, 16-byte blocks, and 32-bit physical address, instead of a direct-mapped cache. Fill in the address breakdown table for this cache with the following **fields:** Index, Tag, and Byte offset and their **corresponding address bits**.

Problem 6

Describe the operation of a data cache. Your description should include discussion of the following:

A) Spatial and temporal locality.
B) Valid bits.
C) Direct mapped versus set-associative structures. Show how cache indexing and tag match works for both direct mapped and 2-way set-associative cache configurations assuming one word per

cache line. What are the advantages and disadvantages of direct mapped versus set-associative structures?

D) Multiple-word cache lines. What are the advantages and disadvantages of multiple- word cache lines? Describe how they are implemented for a direct mapped cache.

E) LRU and random replacement policies. What are their relative advantages and disadvantages?

Problem 7

Examine how pipelining affects the clock cycle time of the processor. Let us assume a processor where the individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
45%	20%	20%	15%

A) What is the clock cycle time in a pipelined and non-piplined processor?
B) What is the total latency of a ***load*** instruction in a pipelined and non-pipelined processor?
C) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?
D) Assuming there are no stalls or hazards, what is the utilization of the data memory?
E) Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

Problem Ratings

problem		A	B	C	D	E	F	G
	1							
	2							
	3							
	4							
	5							
	6							
	7							

0	No idea
1	Used to know it
2	Know it