EC 513
Computer Architecture

On-chip Networking

Prof. Michel A. Kinsky
Virtual Channel Router

Routing Computation

Virtual Channel Allocator

Switch Allocator

Input Ports

VC<sub>0</sub>

VC<sub>x</sub>

VC<sub>0</sub>

VC<sub>x</sub>
What’s In A Router?

- It’s a system as well
  - Logic – State machines, Arbiters, Allocators
    - Control the movement through router
    - Idle, Routing, Waiting for resources, Active
  - Memory – Buffers
    - Store flits before forwarding them
    - SRAMs, registers, processor memory
  - Communication – Switches
    - Transfer flits from input to output ports
    - Crossbars, multiple crossbars, fully-connected, bus
Network Deadlock

- Flow A holds u and v but cannot make progress until it acquires channel w
- Flow B holds channels w and x but cannot make progress until it acquires channel u
Channel Dependency Graph

- Can create a channel dependency graph (CDG) of the network

Vertices in the CDG represent network links

Disallowing 180° turns, e.g.,
AB → BA
Cycles in CDGs

- The channel dependency graph $D$ derived from the network topology may contain many cycles.

Flow routed through links $AB$, $BE$, $EF$.
Flow routed through links $EF$, $FA$, $AB$.
Deadlock!
Key Insight

- If routes of flows conform to acyclic CDG, then there will be no possibility of deadlock!

Disallow/Delete certain edges in CDG

Edges in CDG correspond to turns in network!
Acyclic CDGs

Turns could be prohibited ad-hoc, all the edges in red are deleted

Ad-hoc Acyclic CDG
Turn Model (Glass and Ni, 1994)

- A systematic way of generating deadlock-free routes with small number of prohibited turns
- Deadlock-free if routes conform to at least ONE of the turn models (acyclic channel dependence graph)

West-First Turn Model

North-Last Turn Model
Turn Model Based Acyclic CGD

Per the North-Last prohibited turns, all the edges in red are deleted.
Virtual Channel Based Deadlock Freedom

- Virtual channels can be used to avoid deadlock
Virtual Channel Based Deadlock Freedom
On-Chip Network Routing

- Oblivious Routing
- Statically determined given the source and destination addresses

(+): Simple and fast router designs
(-): Lead to network underutilization
(-): Lack proper load balancing

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XY Routing

<table>
<thead>
<tr>
<th>Link</th>
<th>Capacity</th>
<th>75 Mbytes/sec</th>
</tr>
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<tbody>
<tr>
<td>Each flow</td>
<td>25 Mbytes/sec bandwidth demand</td>
<td></td>
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Adaptive Routing

- Routes dynamically adjusted based on network status
  (+) Better load balancing and path diversity
  (+) Potentially better throughput and latency
  (-) Need for global or local knowledge of network conditions
  (-) Router complexity
Valiant’s Routing Algorithm

- Randomized Routing
  - A packet, going from node SA to node DA, is first routed from SA to a randomly chosen intermediate node IA, before going from IA to final destination DA.
  - It helps load-balance the network and has a good worst-case performance at the expense of locality.
ROMM Routing

- ROMM: Randomized, Oblivious Multi-phase Minimal Routing
  - In an effort to retain locality in routing of packets, the intermediate node is confined to a minimal quadrant
  - This approach essentially translates into randomly selecting between the various minimal paths from the source to the destination
O1TURN Routing

- Orthogonal One-Turn Routing
  - O1TURN: Restricted version of ROMM routing where the intermediate node is one of the corners of the minimum quadrant
  - O1TURN allows each packet to traverse one of at most two routes with equal probability
Modern Computer Architecture Components

- Processing Cores
- Memory Subsystem
- On-chip Interconnect
Next Class

- Project Activities