Multicore Architecture for Control and Emulation of Power Electronics and Smart Grid Systems

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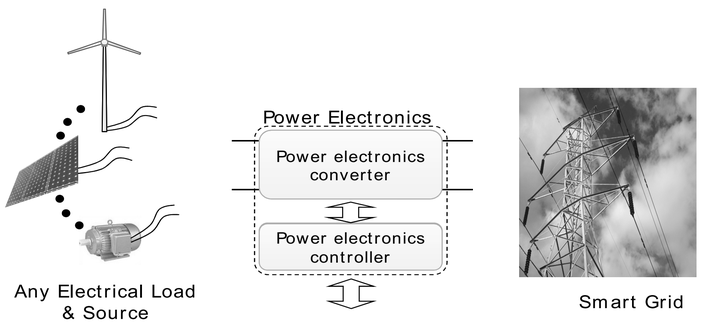
Power Electronics

Power electronics is broadly defined as a solid-state energy conversion technology that enables efficient and agile processing and control of electrical power. The key elements of power electronic circuits are: electronic (solid-state) switches and energy storage elements on one side, and control subsystem on the other side.



Power electronics enables power flow interface of solar photovoltaic with the grid. It provides an efficient interface between variable speed wind turbines and the grid that enables maximum wind power conversion. It allows for power flow control between an electric vehicle motor and battery. It enables power grid dynamic stabilization.

An adequate design, testing, and validation of power electronics systems could potentially reduce overall electricity consumption by more than 30%.

Challenges in Design Automation of Power Electronics

The level of automation in the design, prototyping, verification and testing of power electronics systems is, in many aspects, in the early stages of development. Especially if we compare EDA for power electronics, with for example, with EDA for integrated digital circuit design.

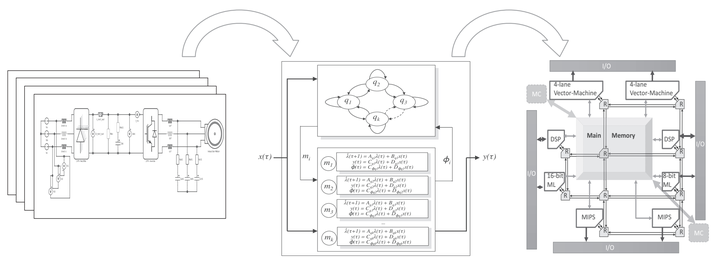
The current design process exhibits several limitations that can be summarized as follows:

- Non-unified design platforms for power and control part.
- Use of time-consuming off-line simulations (time-domain) that partially cover the parameter and design space.
- Lack of well defined design process interfaces.
- Lack of rapid prototyping tools for both hardware and control subsystems.
- Inadequate real-time control system verification and testing, and poor test coverage against faults, parameter variations, etc.
- Lack of rapid prototyping tools for both hardware and control.

An appropriate design and testing of power systems has to incorporate high-fidelity, real-time emulation of power electronics in Hardware-in-the-Loop (HiL) configurations. HiL permits proper validation of operational scenarios by interfacing the platform with other physical systems needed to model the environment.
The validation includes the ability to check system responses and interfaces, to identify failure modes, and to implement recovery states or redundancies in critical circuits.

Our Proposed Design Flow for Power Electronics

Our design framework uses new abstractions and modeling approaches that allows various power electronics applications to be expressed under one general hybrid formulation.
It is a software/hardware co-design environment. The software tool models electrical circuits as switched hybrid automata, analyzes, syntheses, and maps them onto a novel parallel computing hardware.



The computing engine architecture, specifically tailored for high-performance and deterministic real-time computation, enables high-efficiency execution of switched hybrid models of a large class of power electronics systems.

Particular emphasis, in terms of application space and experimental verification, is placed on ultra-low latency, deterministic, and high-throughput computation for power electronics and smart grid systems.

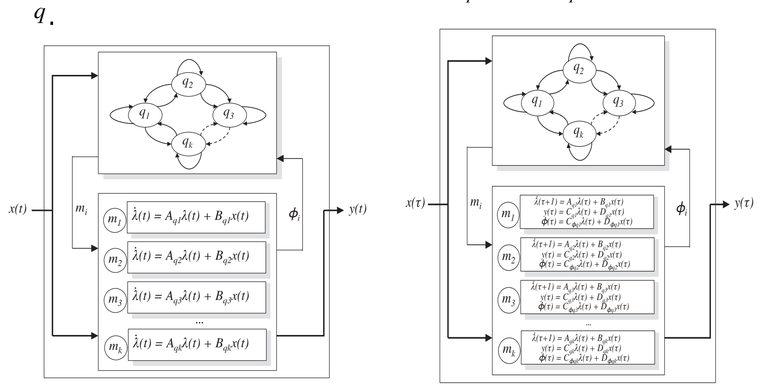
Circuit models are expressed as switched hybrid models which can be executed on a single hardware platform.

Modeling of Power Electronics as Switched Hybrid Automaton

By their very nature, power electronics systems are hybrid systems since they consist of a combination of discrete and continuous features. As such, they are best formalized as hybrid automata (HA). The general behavior of a hybrid automaton consists of discrete state transitions and continuous evaluation. HA provide a natural modeling formalism for power electronics.

Definition 1: We define a switched hybrid system to be a 6-tuple $H = (Q, \Lambda, f, E, I, \Phi)$ where: $Q = \{q_1, ..., q_k\}$ is set of discrete states, $\Lambda \subseteq R^k$ is the continuous state space; $f : Q \mapsto (\Lambda \mapsto R^k)$ assigns to every discrete state a continuous vector field on Λ; $E \subseteq Q \times Q$ is the set of discrete transitions; $I : E \mapsto 2^{\Lambda}$ assigns each transition $e = (q_i, q_j) \in E$ a guard $\phi_e \in \Phi$.
The switched hybrid system model is given in state space form as: $\dot{\lambda}(t) = A_q \lambda(t) + B_q x(t)$.

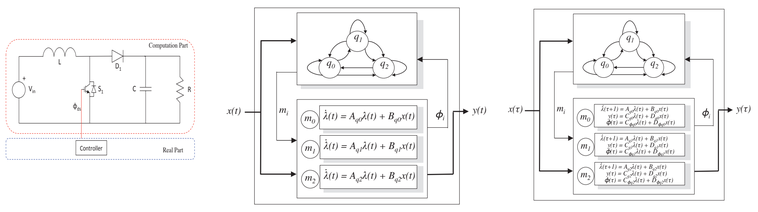
Definition 2: In this framework we also define a system-mode, denoted m_q, where $q \in Q$, to be the operation of the system defined by given state space $\dot{\lambda}(t) = A_q \lambda(t) + B_q x(t)$ and a given q.



Switch hybrid modeling Discretized switch hybrid modeling

Boost Converter Circuit Switch Hybrid Modeling

The boost converter is a high efficiency DC/DC switching-mode power converter, with an output DC voltage greater than its input DC voltage.



Schematic diagram switching states Discretized switched

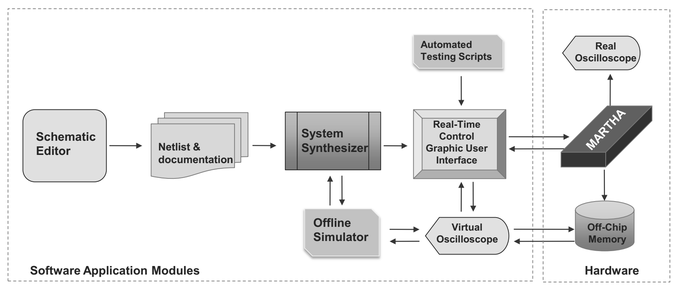
Software Toolchain Support

The software environment has three layers, namely, the power electronics modeling layer, formulation and analysis layer, and the synthesis and simulation layer.

1. Schematic Editor gives designers the ability to convert their power electronics systems specification into model representations, where they can capture component values, connectivity, and characteristics.

2. System Synthesizer which generates the set of matrices representing the discrete states of the power electronics systems, transition equations, control functions, and output signals. The synthesizer output files can be fed either through the offline simulator, or through the real-time controller to be mapped onto the the hardware.

3. Real-Time Control Graphic User Interface performs the mapping of the power electronics system onto the hardware, depending on switching blocks and component blocks signal communications. This mapping consists primarily of loading state-space equation matrices and transition data to memory, emulation execution bit files onto cores, and on-chip network configuration bits.

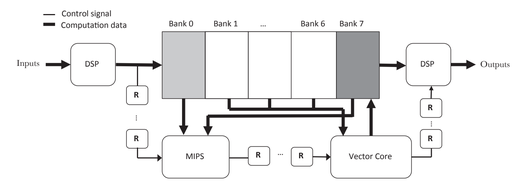


The switched hybrid automaton approach to modeling of power electronics circuits exhibits deterministic and bounded-time execution. One of the drawbacks of this approach is the exponential growth of the number of discrete modes, so in the System Synthesizer, larger complex circuits are partitioned the circuit into subcircuits that communicate via slowly changing state space variables (e.g., capacitor voltage).

Multicore Architecture for Real-Time Hybrid Applications

The MARTHA multicore processor efficiently integrates support for predictable execution-time while providing high-performance and programmability for power electronics applications, smart grid systems, and potentially other hybrid real-time applications.
The MARTHA architecture includes:

- SIMD vector machine style core(s), used to model linear dynamics of power electronics, with fast, parallel, matrix manipulation operations.
- General-purpose MIPS-core(s), used for mode transitions, controls, monitoring, and data collection.
- DSP core(s), used for I/O conditioning, analog/digital communication, and for non-linear machine models.
- Programmable micro-core(s), employed to model certain signal sources, and to implement on-chip control functions.



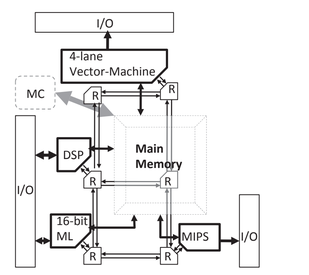
A system-step or time-step is simply the real time interval it takes to associate to a set of inputs the proper set of outputs.

Micro-Architecture of MARTHA-I & MARTHA-II

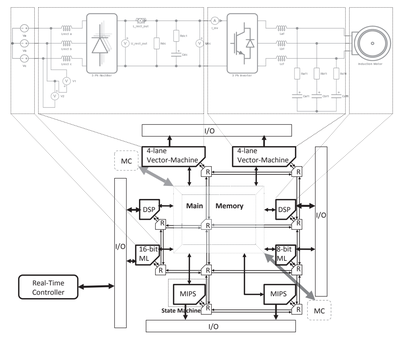
The two versions are intended to show the scalability of the MARTHA architecture, and how subsystem parallelism can be supported.

- MARTHA-I comprises: one reduced instruction set computing (MIPS) core, one four-lane chained vector core for fast and parallel matrix computation, one digital signal processor (DSP), one 16-bit programmable microprocessor, one 8-bit programmable microprocessor, one memory controllers for off-chip communication, and one eight-bank main memory.

- MARTHA-II comprises: two MIPS cores, two four-lane chained vector cores, two DSPs, one 16-bit programmable microprocessor, one 8-bit programmable microprocessor, two memory controllers, and one eight-bank main memory.



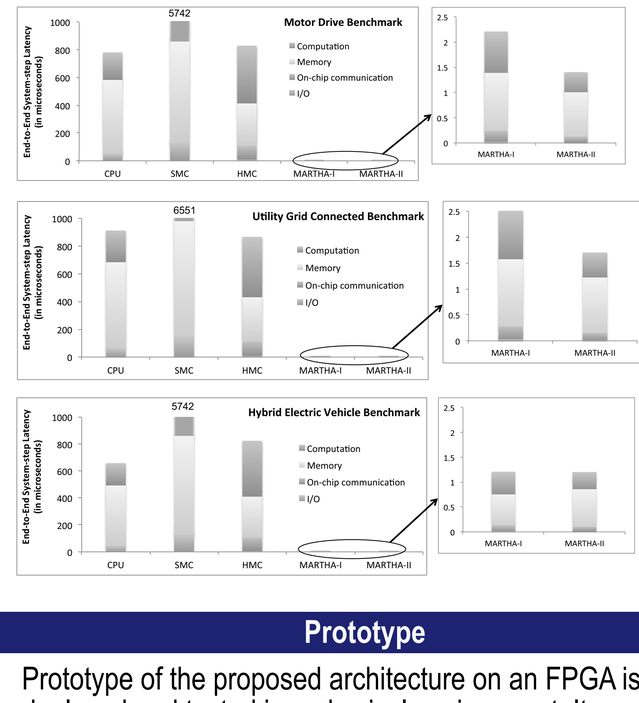
MARTHA-I



MARTHA-II

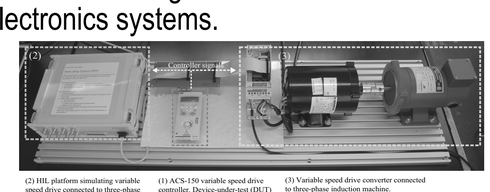
Evaluation

Benchmarks for power electronics are:
1. Variable speed induction motor drive
2. Utility grid connected photovoltaic converter system
3. Hybrid electric vehicle motor drive



Prototype

Prototype of the proposed architecture on an FPGA is deployed and tested in a physical environment. It enables a high-fidelity (with 1s latency and emulation time-step), safe, and fully realistic testing and validation of detailed aspects of power electronics systems.



(2) HIL platform simulating variable speed drive connected to three-phase (1) ACS-150 variable speed drive controller. Device-under-test (DUT) (3) Variable speed drive converter connected to three-phase induction machine.